Appendix A
Example Planar Overview

A.1 The Collateral Material

The information in these appendixes are for reference only, and consists of example planar design information, example firmware, and additional information. It is believed to be correct, but is presented as is, and may contain errors. It is intended to help companies develop their own products using the MCM.

The example planar, along with the firmware and additional information, can be used:

- As a development system.
- To test new boot code, operating systems and/or applications.
- For performance measuring.

The example planar and firmware are:

- Tested for functionality to the level of software internal to IBM as of 12/31/96.
- Prototypes, which may contain prototype ASICs, errata, and/or wiring changes. The example planar may also have errata.

The example planar and firmware are not:

- A fully debugged, complete, and market ready design
- Tested for compliance to FCC and other regulatory requirements
- Intended to be used as a product.
- Sold by IBM.

A.2 Example Planar

In order to offer more robust support to the MCM user, IBM has designed an example planar for the MCM (see Figure A-1). The example planar is described (schematics, BOM, mechanical drawings, and functional information) in these appendixes. The example planar is a working design that is in use internally at IBM, and that was used in the design and development of the MCM.

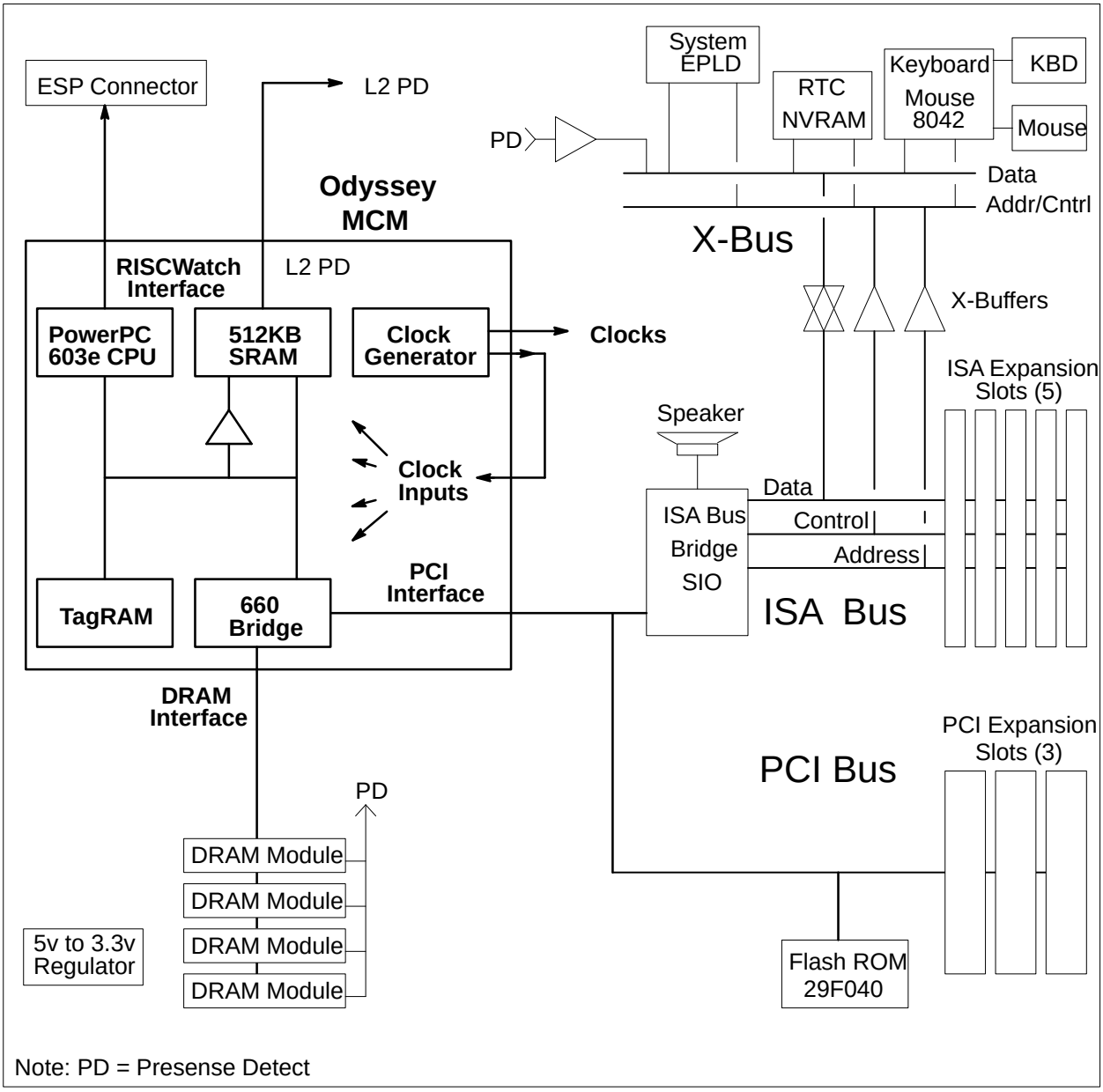


Figure A-1. 100 MHz PPC 603e Example Planar Block Diagram

The example planar is designed to an industry standard BabyAT (8.6 in. by 13 in.) form factor, although the enclosure may need to be modified to provide additional cooling and/or additional space for I/O cards. It requires +5V to power most of the components. The motherboard also requires $\pm$12 V to support some of the peripheral features. Components

that require +3.3V (such as the PCI bus agents) are supported using a regulator mounted on the motherboard to convert +5V to +3.3V. It is sized to fit within a BabyAT form factor enclosure.

A.2.1 System Memory

The example planar memory subsystem can support up to 128M of DRAM memory on four 72 pin modules via sockets. Each SIMM socket can support an 8M or 32M 72 pin SIMM. The DRAM subsystem is 72 bits wide: 64 data bits and eight parity bits. One parity bit is generated for each byte of data written. The MCM can also be configured to perform ECC memory data checking and correction using the same standard parity DRAM modules. Or it can be configured to disable DRAM parity checking for systems using non-parity DRAM.

A.2.2 PCI Bus

The MCM includes the interface between the PCI bus and the rest of the system. The example planar provides three standard PCI expansion slots.

A.2.3 Flash ROM

The example planar uses an AMD AM29F040-120 Flash™ ROM to contain the POST and boot code. Vital Product Data (VPD) such as the motherboard speed and native I/O complement be programmed into in this device. It is possible to program the Flash before or during the manufacturing process.

A.2.4 ISA Bus

The ISA bridge function is provided by an Intel 82378ZB chip (SIO). It provides a PCI to ISA bus bridge where the native I/O and the ISA slots reside, and it provides system services such as ISA bus DMA, PCI bus arbitration, and interrupt control. The example planar provides five PCI expansion slots.

A.2.5 System I/O EPLD

The system I/O EPLD is a programmable logic device that uses the X-bus signals and the partial decode signals from the SIO to decode chip selects for various components.

A.2.6 X–Bus Agents

The example planar uses a Dallas Semiconductor™ DS1385S to provide the real time clock (TOD or RTC) function. This device is PC compatible and resides on the X-bus. It features an additional 4K of NVRAM and a replaceable battery.

The example planar uses an Intel 8042AH as a keyboard and mouse controller.

A.2.7 Power Management

Some components are included on the example planar which can be used for power management hardware. Power management is not implemented on the example planar, and is not intended to be a feature of the example planar.

A.3 Other Help

Several other system, firmware, and miscellaneous issues of interest to the designer are included here. For more information, refer to the IBM PowerPC World Wide Web pages at http://www.chips.ibm.com and ftp://ftp.austin.ibm.com/pub/PPC_support. Also contact your IBM PowerPC Embedded Processor Solutions Technical Representative for details.

Consult specific manufacturer technical specifications for information on specific I/O devices such as hard drives, CD–ROMs, L2 cache cards, video cards, etc. that comprise a total system.

A.3.1 Example Firmware

IBM has developed firmware to support the MCM and example planar. The source code and the binary of this boot & POST firmware is available from IBM. Recommendations in this document for memory mappings, and various software issues may vary from the algorithms implemented in boot code or operating systems.

A.3.2 Design Files

The Gerber format physical design files of the example planar are available from IBM.

A.3.3 Quickstart Peripheral List

The example planar is intended to use typical PC peripherals. Products from a large number of manufacturers should work satisfactorily.

Table A-1 outlines generic requirements for peripherals and gives examples of some devices that have been used for testing. It is not a recommendation of any particular vendor. Table A-1 does not include cables for a parallel port, indicators, a switch, or a speaker.

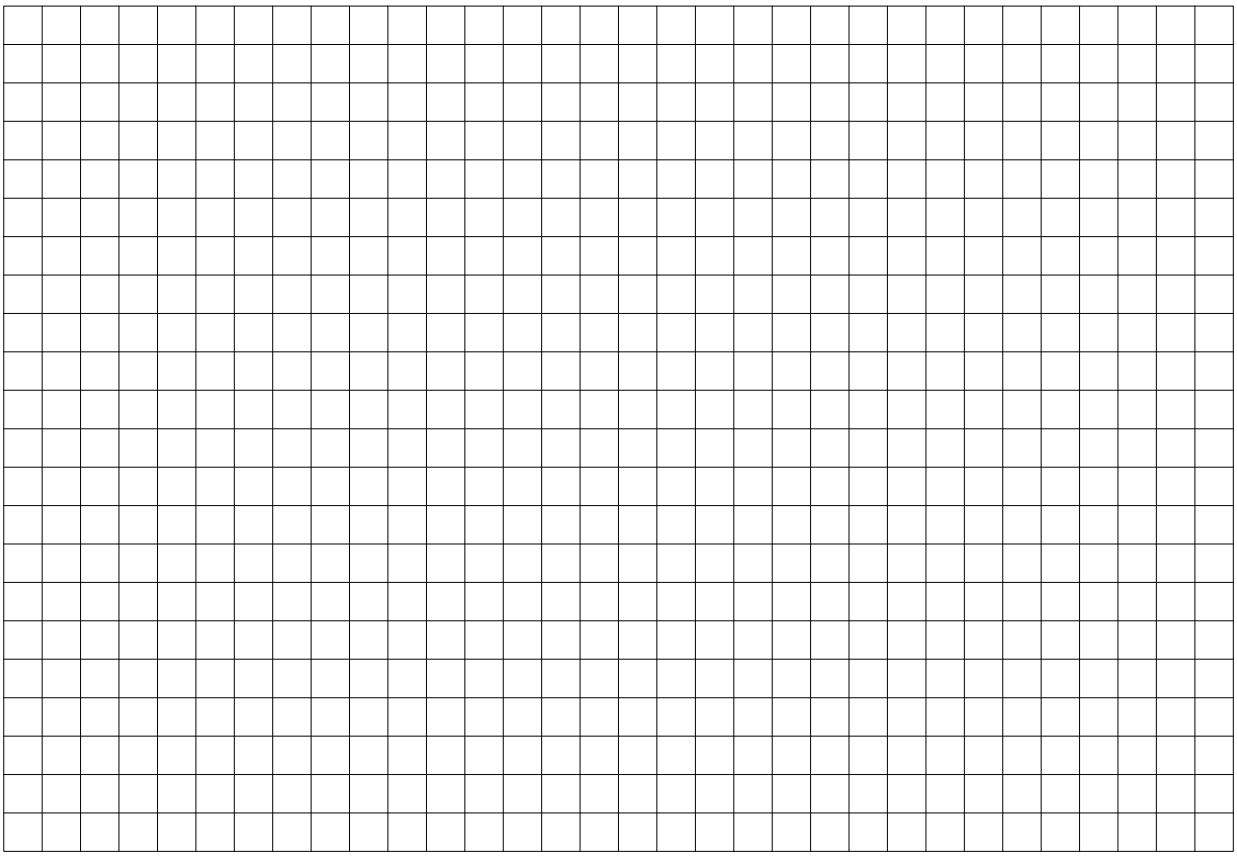
An IBM 3101 asynchronous terminal or equivalent is required for testing with the Bring Up Driver (BUD) code. Settings are 8-bit, no parity, one stop bit, and 9600 baud. VT100 or VT52 emulator terminals may work. It is desirable to also have a video monitor for BUD tests. The boot code will boot with either an async console, a video on motherboard, or both.

Table A-1. Quickstart Peripheral List

Generic Description	Example Device
L2 SRAM card, 256KB	Alliance Semiconductor AS7M64P3256–15C
Loctite 384 adhesive, 300ml cartridge	Loctite Corp. 17041
Loctite 384 activator, 10 liter can	Loctite Corp. 17101
Video adapter card, PCI S3	Diamond Stealth (S3) 864
SCSI adaptor card, PCI	NCR 8100S with 609–039–1635 controller
Super I/O adaptor (IDE, floppy, serial ports, parallel ports, etc.)	Acculogic sIDE–4/HP (110–00139–00E00)
Audio adaptor card	Creative Labs Soundblaster 16
Floppy disk drive, 3.5”x1.44MB	Alps DFR723F, IBM 73G4514, Mitsubishi MF355F–258UG
Hard disk drive, SCSI–2, 8 bit	Quantum LPS270/5405, Maxtor MXT–540SL, IBM WDS–3200 (79F4042)
Hard disk drive, SCSI 1GB	IBM 94G3187
Hard disk drive, IDE 1GB	Maxtor HDMC71260AC
CD_ROM drive, internal SCSI	Toshiba XM–4101BMY
CD_ROM drive, internal SCSI, 4x	Toshiba 5301–4x
CD_ROM drive, internal IDE, 4x	Chinnon CDS5451

Table A-1. Quickstart Peripheral List (Continued)

Generic Description	Example Device
Chassis, Baby AT	Olsen Metal Products CC300249–17
Power supply, 200W Energy Star	API-3186S, IBM 06H2968
Box fan	Panaflow FBA08T12M
Box fan shock mounts	IBM 81F7977
Internal cables, floppy, SCSI, and CD–ROM	Standard cables
Speaker, internal 8Ω .5W 2pin	
LED, 2.5 ma drive	
Asynchronous terminal	IBM 3101
Super VGA monitor	IBM 6324, 6325, 6327, 9524, 9525, 9527, 9521
Keyboard, PS/2 compatible	
Mouse, PS/2 compatible	



Appendix B
Planar I/O Subsystems

B.1 ISA Subsystem

The 100 MHz PPC 603e MCM example planar includes an ISA bus that is interfaced to the PCI bus by the ISA bus bridge. ISA expansion slots are provided by the example planar. The example planar uses a buffered subset of the ISA bus, called the X-bus, to host on-board native I/O, such as the real time clock and the keyboard and mouse controller.

B.1.1 The ISA Bridge

The ISA bridge function is provided by an Intel 82378ZB chip (SIO). It provides a PCI to ISA bus bridge, with the following major functions:

- Bridge between PCI and ISA
  - 8/16 bit ISA devices
  - 24 bit addressing on ISA
  - Partially decodes native I/O addresses
  - Unclaimed PCI memory address below 16MB forwarded to the ISA bus
  - Unclaimed PCI I/O address below 64K forwarded to the ISA bus
  - Powers up to an open condition (i.e., cycles may be passed to the ISA bus)
  - Generates ISA clock, with a programmable divide ratio of three or four
  - Allows ISA mastering and has programmable decodes that map ISA memory cycles to the PCI bus
  - 32–bit posted memory write data buffer (no I/O buffering)
- Seven channel ISA DMA controller
  - Function of two 83C37s with 32–bit extensions
  - Supports 8– bit or 16–bit devices on the ISA bus
  - Supports 32–bit addressing for ISA to PCI memory transfers
  - 8–byte bidirectional buffer for DMA data
- Timer block (function of 82C54)
- Interrupt Controller (function of two 8259s)
- PCI bus arbiter.
- Functions as PCI target during programming and ISA target cycles, and as busmaster during DMA or ISA master cycles

- Generates ISA_REFRESH# signal to refresh ISA bus DRAM.

B.1.2 Address Ranges

The ISA bus address ranges which may be separately enabled in the ISA bus bridge for forwarding to the PCI bus are:

- 0 - 512K
- 512K - 640K
- 640K - 768K
- 768K - 896K (in 8 ranges of 16 K each)
- 896K - 960K
- 1M - xM (where $x \leq 16$) with the hole (see the SIO data book). The hole may be 64K or 8M.

If an ISA DMA produces an address in the 0-16M range and this address is enabled in the ISA bridge for forwarding to the PCI, the ISA bridge will initiate a PCI transaction which the 660 bridge will forward to system memory.

The 660 uses medium timing when claiming ISA master originated cycles on the PCI. It does not use subtractive decoding. Hence, ISA masters can only communicate with other ISA devices or system memory. They may not communicate with PCI devices.

Warning: The software should not map any PCI memory at PCI addresses which ISA masters can create (those addresses between 0-16M which are programmed for forwarding from ISA to PCI). This is because contention would result between the device mapped at that address and the 660. Alternatively stated, ISA masters should not be allowed to create accesses to system memory using any address between 0 and 16M that is mapped to a PCI device, such as video.

B.1.3 ISA Bus Concurrency

ISA bus cycles which are not enabled for forwarding, including the hole, remain on the ISA bus. That is, DMA or ISA busmaster cycles on the ISA bus can run concurrently with PCI or CPU cycles.

B.1.4 ISA Busmasters and IGN_PCI_AD31

The ISA bridge supports ISA busmasters. System memory accesses from an ISA busmaster are designed to be mapped to the 0 to 16M range, and the ISA bridge forwards them to the PCI bus at the same range, which is not compliant to the PowerPC Reference Platform specification. Other PCI to system memory accesses however, are correctly mapped to the 2G to 4G range (for system memory address range from 0 to 2G). In some architectures this problem is handled by using the ISA_MASTER# signal, which is active during the ISA busmaster operation.

However, the ISA bridge allows ISA masters to run posted writes to system memory, without latching in the accompanying ISA_MASTER# signal. In this situation, the ISA_MASTER# signal is no longer synchronized to the ISA busmaster operation.

To overcome this challenge, the example system detects PCI memory transactions that are initiated by the SIO. The example planar ANDs together GNT0#, GNT1#, and GNT2#, to generate IGN_PCI_AD31, which is active high during the address phase of any PCI transaction that is not initiated by one of the three possible PCI agents (besides the 660 and the SIO). If the PCI transaction was not initiated by the 660, and if it is a memory transaction, then the 660 assumes that it is a system memory transaction initiated on the PCI bus by the SIO on behalf of an ISA busmaster, and so forwards it to the correct system memory address in the 0 to 16M range.

As a consequence of this design, the ISA bridge must be programmed to map ISA DMA (that is bound for system memory) to a PCI memory transaction using the 0 to 2G address range, rather than the apparently correct 2G to 4G range. Since the DMA sourced PCI transaction also causes IGN_PCI_AD31 to be asserted during the address phase of a PCI transaction initiated by the ISA bridge, the 660 will not do the usual inversion of the highest order address bit, but will forward the transaction to system memory in the 0 to 2G range.

Another consequence of the design is that the ISA bridge can not initiate peer to peer PCI memory transactions, because no matter what the PCI address is, it will be claimed by the 660 (if the address is that of a populated memory location) and mapped to system memory, possibly causing various inappropriate results.

These are the only limitations on the normal operation of the ISA bridge that are caused by the IGN_PCI_AD31 design, and there are no implications for other PCI or ISA agents, which are totally unaffected by the situation.

B.1.5 DMA

The DMA controller in the ISA bridge consists of the functionality of two 82C37A DMA controllers with 32-bit addressability extensions and enhanced functionality. The DMA request/grant lines are connected on the example planar as shown in Table B-1.

Table B-1. DMA Assignments

DMA Channel	Assignment or Connection
0	ISA connectors
1	ISA connectors
2	ISA connectors
3	ISA connectors
4	Cascade in
5	ISA connectors
6	ISA connectors
7	ISA connectors

B.1.5.1 Supported DMA Paths

DMA operations can be performed only:

- From ISA I/O mapped devices to ISA memory mapped devices, and
- From ISA I/O mapped devices to system memory (via the PCI bus). In these transfers, the system memory address must be mapped to the PCI address range 0 to 2G (see Section B.1.4).

The DMA source device can be located on the X-bus. If the DMA target is ISA memory mapped, it can also reside on the X-bus.

- ISA DMA to PCI I/O devices is not allowed.
- ISA DMA to PCI memory devices is not allowed.
- ISA DMA from ISA memory mapped devices is not allowed.

B.1.5.2 DMA Timing

The DMA controller runs compatible cycles for all ISA to ISA DMA transfers. Type A, type B and type F timing is available only for ISA I/O to system memory (via the PCI) DMA transfers.

B.1.5.3 Scatter-Gather

The example planar permits the use of independent scatter-gather (SG) operations on DMA channels 0-3 and 5-7. This operation chains together a number of DMA transfers to different memory locations so that they appear as one DMA transfer. The SG command, descriptor table, and status registers are relocatable via a configuration register in the ISA bridge. The termination of an operation may be signaled to the software by configuring any (or all) of the SG channels to use IRQ13 or by configuring the channel to signal end of process (aka Terminal Count) to the DMA device. See the SIO data book for details.

B.1.5.4 X-Bus

The X-bus is a utility bus, an 8 bit buffered version of the ISA bus, implemented on the reference board to support the native I/O devices that are located on the reference board. X-bus data transceiver U12 is controlled by the ISA bridge via XDIR (UBUSTR) and XDEN# (UBUSOE#). Various devices are located on the X–bus.

B.1.5.5 Control Signal Decodes

The System I/O EPLD (Chandra) is a programmable logic device that uses the X-bus signals and the partial decode signals from the ISA bridge to decode chip selects for various components. For more information on the System I/O EPLD, see that data sheet.

B.1.5.6 Keyboard/Mouse Controller

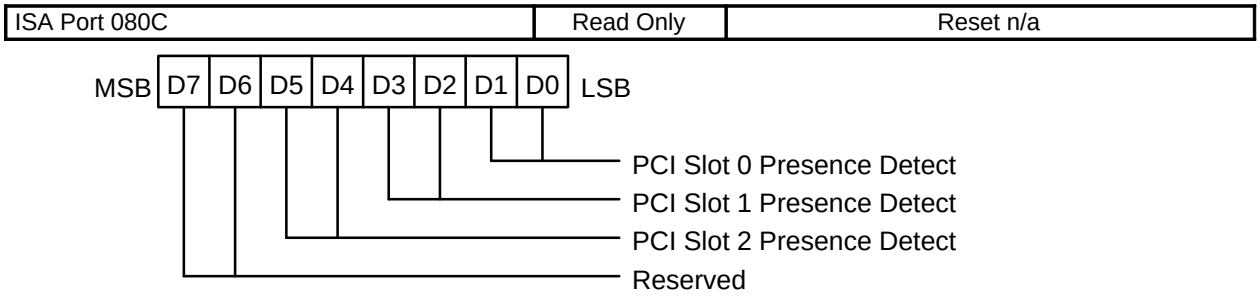
The example planar uses an Intel 8042AH as a keyboard and mouse controller, which resides on the X-bus. The code used is the same version as used in IBM Personal System/2 machines. This microcode may differ from other 8042 type keyboard controllers. These differences are usually only significant when porting AIX to the system (for more information contact your IBM representative. This device contains several registers. See the data sheet for more information.

B.1.5.7 Real Time Clock (RTC)

The example planar uses a Dallas Semiconductor™ DS1385S to provide the real time clock (TOD or RTC) function. This device is PC compatible and resides on the X-bus. It features an additional 4K of NVRAM and a replaceable battery. This device contains several registers. See the data sheet for more information.

B.1.5.8 PCI Adapter Card Presence Detect Register

The example planar uses U20 to buffer the PCI adaptor card presence detection bits onto the X-bus under control of the system I/O EPLD. These bits report in pairs, and do not contain any information about the identity of the card. They merely report on its presence.



Bits 7:6 Reserved

Bits 5:4 PCI Slot 2 Presence Detect Bits. 00 = Present, 11 = No PCI card installed.

Bits 3:2 PCI Slot 2 Presence Detect Bits. 00 = Present, 11 = No PCI card installed.

Bits 1:0 PCI Slot 2 Presence Detect Bits. 00 = Present, 11 = No PCI card installed.

B.1.5.9 L2 SRAM Identification Register

The example planar uses U19 to buffer the SRAM identification/presence detect bits from the SRAM socket onto the X-bus under control of the system I/O EPLD.

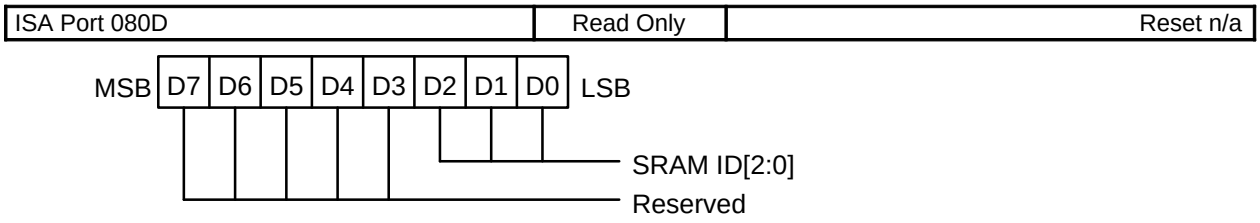


Table B-2. DRAM Module Presence Detect Bit Encoding

SRAM ID [2:0]			SRAM Module Identification
ID3	ID2	ID1	
0	0	0	512K Synchronous
0	0	1	256K Synchronous
0	1	0	Reserved
0	1	1	Reserved
1	0	0	512K Asynchronous
1	0	1	256K Asynchronous
1	1	0	1M Asynchronous
1	1	1	L2 SRAM module not present

B.1.5.10 Planar ID Detection Register

Revision information on the planar (motherboard) is buffered onto the X-bus by U18, under control of the system I/O EPLD.

ISA Port 0852	Read Only	Reset n/a

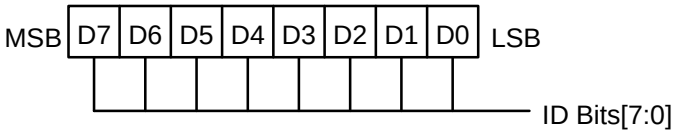


Table B-3. Planar ID Encoding

Planar ID[7:0]	CPU	CPU Internal Clock/ CPU Bus Clock/ PCI Bus Clock	Schematic
0C	603	66/66/33	MPRH02SCU–01
0D	603e	99/66/33	MPRH02SCU–01
0E	604	132/66/33	MPRH02SCU–01
other	—	—	Reserved

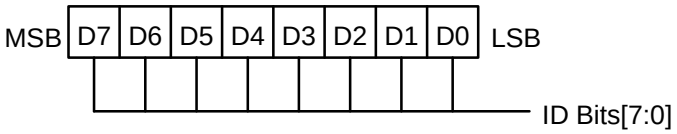
B.1.5.11 DRAM Presence Detection

DRAM module presence and identification data is hard coded into the pinout of the SIMM (or DIMM) by shorting particular pins to ground or no-connecting them on the SIMM itself. The example planar uses U17 and U40 to buffer the presence detect bits from the DRAM sockets onto the X-bus under control of signals from the system I/O EPLD. This information appears as the DRAM SIMM 1-2 Memory ID Register and the DRAM SIMM 3-4 Memory ID Register.

B.1.5.12 DRAM SIMM 1-2 Memory ID Register

ISA Port 0880	Read Only	Reset n/a

This register indicates the ID bits associated with SIMMs 1 and 2.



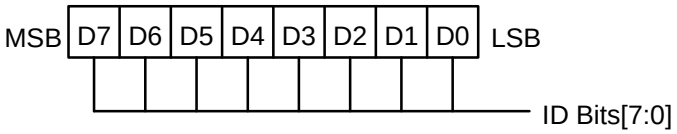
Bits 7:4 SIMM 2 ID bits. See Table B-4.

Bits 3:0 SIMM 1 ID bits. See Table B-4.

B.1.5.13 DRAM SIMM 3-4 Memory ID Register

ISA Port 0881	Read Only	Reset n/a

This register indicates the ID bits associated with SIMMs 3 and 4.



Bits 7:4 SIMM 4 ID bits. See Table B-4.

Bits 3:0 SIMM 3 ID bits. See Table B-4.

Table B-4. DRAM Module Presence Detect Bit Encoding

Presence Detect Bits				DRAM Module Identification
PD4	PD3	PD2	PD1	
1	0	0	0	4 MB (1M x 36b) 70ns
1	0	1	1	8 MB (2M x 36b) 70ns
1	0	1	0	16 MB (4M x 36b) 70ns
1	1	0	1	32 MB (8M x 36b) 70ns
1	1	1	1	No DRAM module installed.
Other encodings				Not currently defined.

B.1.6 Miscellaneous

B.1.6.1 Speaker Support

The example planar has a connector for a small speaker. The speaker output is driven by the timer 2 signal from the ISA bridge. The intended speaker is a typical PC type, 8 ohms and .5W.

B.2 System EPLD

Note: The System I/O EPLD generates system control register access signals from X-bus I/O port transactions, supports power management, and provides various other system functions.

In this section, the system I/O EPLD is referred to as the EPLD.

The EPLD is a programmed Altera™ EPM5130QC100 electrically programmable logic device. For timing and electrical specifications, see that data sheet.

B.2.1 System Register Support

The EPLD supports both internal and external registers.

B.2.1.1 External Register Support

The EPLD supports a group of external registers, which are latches or other devices that are physically located in a device other than the EPLD. As shown in Figure B-1, the EPLD supplies control signals to the external registers, based on a decode of the address and control lines of the X-bus (or ISA bus). In response to the signals from the EPLD, the external register either reads or writes data to the X-bus.

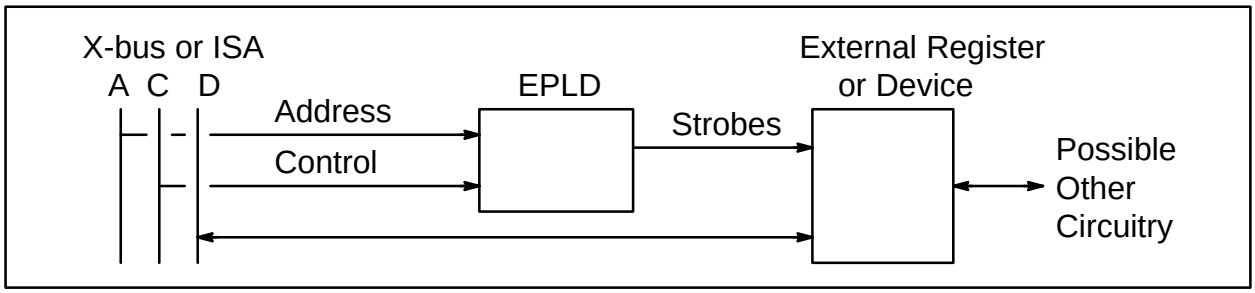


Figure B-1. Typical External Register

For the external registers that the EPLD supports, Table B-5 shows the external register, the ISA I/O port address, and the supplied control signal(s).

Table B-5. External Register Support

ISA Port Address	Register	Read/ Write	Register Location	Signal	Strobe or Function
0060 or 0062 or 0064 or 0066	Keyboard Controller Registers	R/W	Keyboard Controller	KBD_CS# (asserted for an access to any of these addresses)	Address Decode
0070	RTC Address Latch Enable	W/O	RTC	RTC_ALE	Write strobe
0071	RTC Data	Write	RTC	RTCWR#	Write strobe
		Read		RTCDS#	Read strobe
0074	NVRAM Address Low Byte	W/O	NVRAM	AS0#	Address Decode
0075	NVRAM Address High Byte	W/O	NVRAM	AS1#	Address Decode
0077	NVRAM Data	Write	NVRAM	NVRAMWE#	Write Strobe
		Read		NVRAMOE#	Read Strobe
080C	Equipment Present	R/O	Board	PRSNT_RD#	Read Strobe
080D	L2 Cache Status Register	R/O	Board	L2_STATUS_RD#	Read Strobe
0852	Planar ID	R/O	Board	PLANAR_ID_RD#	Read Strobe
0880	DRAM Presence Detect 1/2	R/O	Board	DRAM_PD_RD1#	Read Strobe
0881	DRAM Presence Detect 3/4	R/O	Board	DRAM_PD_RD2#	Read Strobe

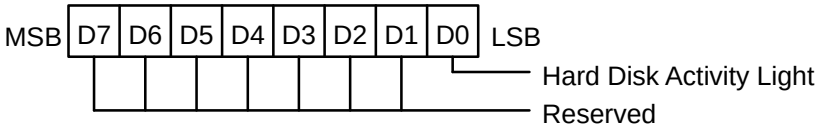
B.2.1.2 Internal Registers

The EPLD contains a group of internal registers, which are accessed via the ISA bus I/O port address shown for each register.

Storage Light Register

ISA Port 0808	Read/Write	Reset to xxxx xxx0

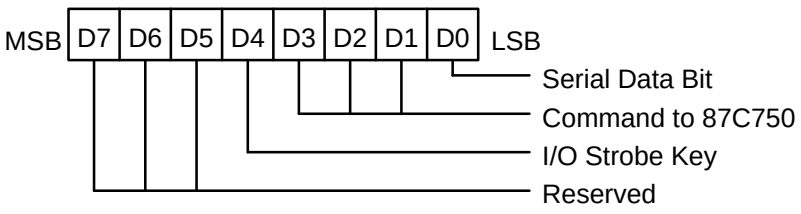
This register controls the HDD_LED# output of the EPLD. This signal normally controls the hard disc drive activity LED.



Bit 0 . . . Hard Disk Activity Light:
0 = Turn light off (negate HDD_LED#).
1 = Turn light on (assert HDD_LED#).

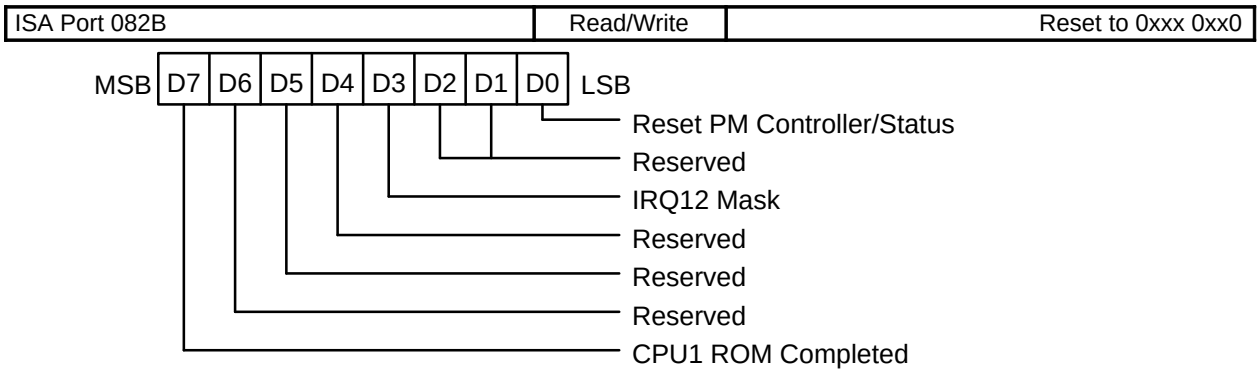
Power Management Control Register 1

ISA Port 082A	Read/Write	Reset to xxxx xxxx



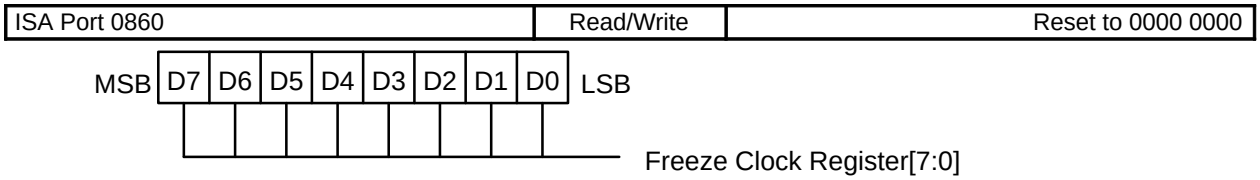
This register is part of the power management system. For a detailed functional description of the operation of this register, see the *603/604 Reference Design Power Management Specification*.

Power Management Control Register 2



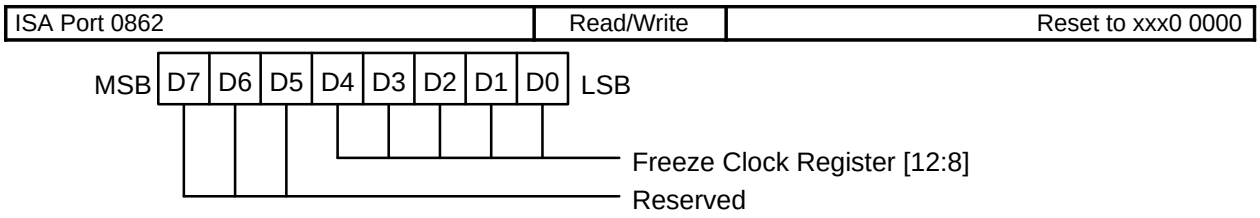
This register is part of the power management system. For a detailed functional description of the operation of this register, see *The 603/604 Reference Design Power Management Specification*.

Freeze Clock Register (FCR) Low



See FCR high.

Freeze Clock Register (FCR) High



The freeze clock register (FCR) is a 13 bit register that is accessed by the system via the X-bus as two 8-bit registers, as shown in this and the previous sections. Once triggered, the FCR data is shifted out as serial data on FRZ_DATA_OUT.

This function is intended for use with the MPC970 clock chip, as is done in the example planar. The MPC970 contains an input shift register, the input of which (Frz_Data) is connected to FRZ_DATA_OUT. ISA_CLK is used to clock the data from the EPLD to the MPC970.

EPLD will shift the freeze clock data out of the FCR in response to either one of two triggers:

1. A write to ISA I/O port 862, or

2. A low to high transition on the UNFREEZE input iff bit 0 and bit 1 of the FCR are high.

After triggering the data transfer, wait at least 2.3us for the transfer to complete before accessing the FCR or retriggering the data transfer.

This is a one way serial data transfer between the two devices. Reading the FCR returns the contents of the FCR, and does not cause a read of the data in the MPC970 register.

A 1 in a bit position freezes the corresponding clock output of the MPC970. For details of the data transfer operation and the meaning of the data, see the MPC970 data sheet.

B.2.2 Signal Descriptions

Table B-6 shows the active signals of the EPLD. Pins not shown should not be connected.

Table B-6. Signal Descriptions

Signal Name	Pin	I/O	Description
X-bus Interface Signals			
ECS[2:0]	21, 22, 59	I	Encoded Chip Select [2:0]. Encoded chip selects for peripheral devices supported by the ISA I/O Bridge. Used by EPLD X-bus I/O port address decoders. From SIO.
ECSEN#	60	I	Encoded Chip Select Enable. Asserted to enable the base decoder. Negated to select the option decoder. Used by EPLD X-bus I/O port address decoders. From SIO.
XA[7:0]	61 ,64, 65, 66, 67, 70, 71, 72.	I	X–address bus [7:0]. Used by EPLD X-bus I/O port address decoders.
XD[7:0]	31, 32, 33, 92, 73, 74, 34, 95.	I/O 24mA	X-data bus [7:0]. Used by EPLD to transfer data.
XIOW#	16	I	X-bus I/O Write. This signal indicates that the system is writing to an X-bus I/O device. Used by EPLD X-bus I/O port address decoders.
XIOR#	9	I	X-bus I/O Read. This signal indicates that the system is reading from an X-bus I/O device. Used by EPLD X-bus I/O port address decoders.
External Register Support Signals			
AS0#	50	O 6mA	NVRAM address register low byte write strobe. EPLD asserts this signal to write to X–bus port 0074.
AS1#	49	O 6mA	NVRAM address register high byte write strobe. EPLD asserts this signal to write to X–bus port 0075.
DRAM_PD_RD1#	57	O 6mA	DRAM SIMM presence detect read enable 1. EPLD asserts this signal to read X-bus port 0880.
DRAM_PD_RD2#	56	O 6mA	DRAM SIMM presence detect read enable 2. EPLD asserts this signal to read X-bus port 0881.
KYBD_CS#	98	O 6mA	Keyboard chip select. EPLD asserts this signal to read X-bus ports 0060, 0062, 0064, and 0066.
L2_STATUS_RD#	54	O 6mA	L2 cache status register read strobe. EPLD asserts this signal to read X-bus port 080D.
NVRAMOE#	1	O 6mA	NVRAM output enable (read strobe). EPLD asserts this signal to read X–bus port 0076. This normally causes a read of the NVRAM data stored at the location contained in the NVRAM address register.

Table B-6. Signal Descriptions (Continued)

Signal Name	Pin	I/O	Description
External Register Support Signals			
NVRAMWE#	53	O 6mA	NVRAM data write strobe. EPLD asserts this signal to write to X–bus port 0076. This normally causes the data associated with this write to be written into the NVRAM location contained in the NVRAM address register.
PLANAR_ID_RD#	52	O 6mA	Planar ID read. EPLD asserts this signal to read X-bus port 0852.
PRSNT_RD#	41	O 6mA	Equipment present register read. EPLD asserts this signal to read X-bus port 080C.
RTC_ALE	48	O 6mA	Real time clock address latch enable. EPLD asserts this signal to write X-bus port 0070.
RTCDS#	51	O 6mA	Real time clock read strobe. EPLD asserts this signal to read X–bus port 0071.
RTCWR#	35	O 6mA	Real time clock write strobe. EPLD asserts this signal to write to X–bus port 0071.
Interrupt Signals			
IRQ1	86	O	Interrupt request 1. Latched active when IRQ1_IN is asserted. Negated when KYBD_CS# is asserted.
IRQ1_IN	89	I	Keyboard interrupt. EPLD is designed to intercept the keyboard interrupt between the keyboard and the ISA bus bridge. Either connect IRQ1 and IRQ1_IN as shown in the example planar schematics, or disconnect both signals from the system (routing the keyboard interrupt to the ISA bus bridge), or see the *603/604 Reference Design Power Management Guide*.
IRQ12	36	I	Interrupt request 12 input. Connect to system IRQ12, the mouse interrupt. Also see the *603/604 Reference Design Power Management Guide*.
System Clock Interface Signals			
FRZ_DATA_OUT	90	O 6mA	Freeze data out. Serial data stream to MPC970 clock chip. See the MPC970 data sheet.
ISA_CLK	20	I	ISA clock. Used to clock the freeze serial data stream to the MPC970 clock chip. See the MPC970 data sheet. Also see the *603/604 Reference Design Power Management Guide*.
Power Management Signals (not used in release 2.0 or 2.1)			
83CX_RESET	91	O 6mA	Power management controller reset. No-connect or connect as shown in the *603/604 Reference Design Power Management Guide*.
ACTIVITY#	58	O 6mA	Activity. No-connect or connect as shown in the *603/604 Reference Design Power Management Guide*.
CMD_STATE#	8	I	Power management controller command state. No-connect or connect as shown in the *603/604 Reference Design Power Management Guide*.
EXT_ACTVTY#	3	I	External activity. No-connect or pull low or connect as shown in the *603/604 Reference Design Power Management Guide*.
IO_STROBE#	99	O 6mA	I/O strobe. No-connect or connect as shown in the *603/604 Reference Design Power Management Guide*.
PROC_RDY	83	I	Power management controller ready. No-connect or connect as shown in the *603/604 Reference Design Power Management Guide*.
RWD0	96	I/O 24mA	Power management controller serial read/write data bit. No-connect or connect as shown in the *603/604 Reference Design Power Management Guide*.

Table B-6. Signal Descriptions (Continued)

Signal Name	Pin	I/O	Description
Power Management Signals (not used in release 2.0 or 2.1)			
UNFREEZE	82	I	Unfreeze. No-connect or connect as shown in the *603/604 Reference Design Power Management Guide*.
Other Signals			
HDD_LED#	100	O 6mA	Hard disk drive activity light. EPLD asserts this signal while bit 0 of the storage light register (port 0808) is 1. This signal normally indicates hard disk drive activity.
RESET#	10	I	System reset. Used by EPLD to reset internal state machines and internal registers.
VCC	18, 19, 43, 44, 68, 69, 93, 94	I	+5V:
GND	12, 13, 37, 38, 62, 63, 87, 88	I	GROUND:

B.2.3 EPLD Design Equations

B.2.3.1 Fit File

```
-- MAX+plus II Compiler Fit File
-- Version 5.0 8/5/94
-- Compiled: 05/05/95 14:44:22

BEGIN
    DEVICE = "EPM5130WC-1";
    "A0"                          : INPUT_PIN  = 72     ;
    "A1"                          : INPUT_PIN  = 71     ;
    "A2"                          : INPUT_PIN  = 70     ;
    "A3"                          : INPUT_PIN  = 67     ;
    "A4"                          : INPUT_PIN  = 66     ;
    "A5"                          : INPUT_PIN  = 65     ;
    "A6"                          : INPUT_PIN  = 64     ;
    "A7"                          : INPUT_PIN  = 61     ;
    "/CMD_STATE"                  : INPUT_PIN  = 8      ; -- LC8
    "/ECSEN"                      : INPUT_PIN  = 60     ;
    "ECS0"                        : INPUT_PIN  = 59     ;
    "ECS1"                        : INPUT_PIN  = 22     ;
    "ECS2"                        : INPUT_PIN  = 21     ;
    "/EXT_ACTVTY"                 : INPUT_PIN  = 3      ; -- LC3
    "IRQ1"                        : INPUT_PIN  = 89     ; -- LC103
    "IRQ12"                       : INPUT_PIN  = 36     ; -- LC38
    "ISA_CLK"                     : INPUT_PIN  = 20     ;
    "PROC_RDY"                    : INPUT_PIN  = 83     ; -- LC99
    "/RESET"                      : INPUT_PIN  = 10     ;
    "UNFREEZE"                    : INPUT_PIN  = 82     ; -- LC98
    "/XIOR"                       : INPUT_PIN  = 9      ;
    "/XIOW"                       : INPUT_PIN  = 16     ;
```

```
"/ACTIVITY"          : OUTPUT_PIN = 58     ; -- LC72
"/AS0"               : OUTPUT_PIN = 50     ; -- LC56
"/AS1"               : OUTPUT_PIN = 49     ; -- LC55
"/DRAM_PD_RD1"       : OUTPUT_PIN = 57     ; -- LC71
"/DRAM_PD_RD2"       : OUTPUT_PIN = 56     ; -- LC70
"FRZ_DATA_OUT"       : OUTPUT_PIN = 90     ; -- LC104
"/HDD_LED"           : OUTPUT_PIN = 100    ; -- LC120
"/IO_STROBE"         : OUTPUT_PIN = 99     ; -- LC119
"IRQ1_OUT"           : OUTPUT_PIN = 86     ; -- LC102
"/KYBD_CS"           : OUTPUT_PIN = 98     ; -- LC118
"/L2_STATUS_RD"      : OUTPUT_PIN = 54     ; -- LC68
"/NVRAMOE"           : OUTPUT_PIN = 1      ; -- LC1
"/NVRAMWE"           : OUTPUT_PIN = 53     ; -- LC67
"/PLANAR_ID_RD"      : OUTPUT_PIN = 52     ; -- LC66
"/PRSNT_RD"          : OUTPUT_PIN = 41     ; -- LC49
"RTC_ALE"            : OUTPUT_PIN = 48     ; -- LC54
"/RTCDS"             : OUTPUT_PIN = 51     ; -- LC65
"/RTCWR"             : OUTPUT_PIN = 35     ; -- LC37
"83CX_RESET"         : OUTPUT_PIN = 91     ; -- LC113
"RWD0"               : BIDIR_PIN  = 96     ; -- LC116
"XD0"                : BIDIR_PIN  = 95     ; -- LC115
"XD1"                : BIDIR_PIN  = 34     ; -- LC36
"XD2"                : BIDIR_PIN  = 74     ; -- LC82
"XD3"                : BIDIR_PIN  = 73     ; -- LC81
"XD4"                : BIDIR_PIN  = 92     ; -- LC114
"XD5"                : BIDIR_PIN  = 33     ; -- LC35
"XD6"                : BIDIR_PIN  = 32     ; -- LC34
"XD7"                : BIDIR_PIN  = 31     ; -- LC33
"CLKFF0"             : LOCATION   = LC48   ;
"CLKFF1"             : LOCATION   = LC96   ;
"CLKFF2"             : LOCATION   = LC95   ;
"CLKFF3"             : LOCATION   = LC94   ;
"CLKFF4"             : LOCATION   = LC47   ;
"CLKFF5"             : LOCATION   = LC46   ;
"CLKFF6"             : LOCATION   = LC45   ;
"CLKFF7"             : LOCATION   = LC44   ;
"CLKFF8"             : LOCATION   = LC43   ;
"CLKFF9"             : LOCATION   = LC93   ;
"CLKFF10"            : LOCATION   = LC92   ;
"CLKFF11"            : LOCATION   = LC91   ;
"CLKFF12"            : LOCATION   = LC112  ;
"CNTR0"              : LOCATION   = LC111  ;
"CNTR1"              : LOCATION   = LC110  ;
"CNTR2"              : LOCATION   = LC109  ;
"CNTR3"              : LOCATION   = LC108  ;
"DOUBLE_FRZ"         : LOCATION   = LC90   ;
```

```
    "DOUBLE_SNC"                    : LOCATION   = LC107  ;
    "FREEZEFF"                      : LOCATION   = LC106  ;
    "GEN_STOP_BITFF"                : LOCATION   = LC105  ;
    "GPCS0"                         : LOCATION   = LC89   ;
    "PWR_REG21"                     : LOCATION   = LC80;  --IRQ12_MASK
    "PWR_REG22"                     : LOCATION   = LC79   ;
    "SHIFT_ENFF"                    : LOCATION   = LC103  ; -- PIN 89
    "SNC_FREEZE"                    : LOCATION   = LC99   ; -- PIN 83
    "SNC_SHIFT_ENFF"                : LOCATION   = LC98   ; -- PIN 82
    "SNC_UNFREEZE"                  : LOCATION   = LC101  ; -- PIN 85
    "START_SHIFTFF"                 : LOCATION   = LC100  ; -- PIN 84
    "UNFREEZEFF"                    : LOCATION   = LC97   ; -- PIN 81
END;
```

B.2.3.2 TDF File

```
%*************************************************************************%
%****** AHDL  SOURCE CODE FOR: SIO/XBUS INTERFACE CONTROL  ****************%
%*************************************************************************%

SUBDESIGN chandra(
%%
%        DEFINE PRIMARY INPUTS AND OUTPUTS                              %
%%
   A[7..0]            :INPUT; % A7 is MSB and A0 is LSB  %
   ECS[2..0]          :INPUT; % ECS2 is MSB and ECS0 is LSB  %
   /ECSEN             :INPUT;
   /XIOR              :INPUT;
   /XIOW              :INPUT;
   /RESET             :INPUT;
   /CMD_STATE         :INPUT;
   PROC_RDY           :INPUT;
   /EXT_ACTVTY       :INPUT;
   IRQ1               :INPUT;
   IRQ12              :INPUT;% Freeze Clock  %
   ISA_CLK            :INPUT;
   UNFREEZE           :INPUT;

   /PLANAR_ID_RD      :OUTPUT;
   /PRSNT_RD          :OUTPUT;
   /L2_STATUS_RD      :OUTPUT;
   /DRAM_PD_RD1       :OUTPUT;
   /DRAM_PD_RD2       :OUTPUT;
   /KYBD_CS          :OUTPUT;
   IRQ1_OUT           :OUTPUT;
   RTC_ALE            :OUTPUT;
   /RTCDS             :OUTPUT;
   /RTCWR             :OUTPUT;
   /AS0               :OUTPUT;
   /AS1               :OUTPUT;
   /NVRAMWE           :OUTPUT;
   /NVRAMOE           :OUTPUT;
   /HDD_LED           :OUTPUT;
```

```
   83CX_RESET          :OUTPUT;
   /ACTIVITY           :OUTPUT;
   /IO_STROBE          :OUTPUT;
   FRZ_DATA_OUT        :OUTPUT;

   XD[7..0]            :BIDIR;    % XD7 is MSB and XD0 is LSB  %
   RWD0                :BIDIR;
                                  )

VARIABLE                          % Misc. Variables%
    GPCS0              :NODE;
    HDD_LEDFF          :SRFF;
    D[7..0]            :NODE;
    XD_TRI_OE          :NODE;
    LIGHT_STRB         :NODE;
    INT1FF            :DFF;      % Keyboard interput latch %
    CLRINT1           :NODE;     % Power Management Variables%
    PWR_REG1_STRB      :NODE;
    PWR_REG2_STRB      :NODE;
    PWR_REG2[2..0]     :SRFF;
    83CX_CS            :NODE;
    RWD0_STRB          :NODE;
    IRQ12_MASK         :NODE;     % Freeze Clock Variables %
    CLKFF[12..0]       :DFFE;
    SHIFT_ENFF         :SRFF;
    CNTR[3..0]         :DFF;
    SNC_SHIFT_ENFF     :DFFE;
    START_SHIFTFF      :SRFF;
    CLKFF_WR           :NODE;
    CLKFF_STRB         :NODE;
    CLKFF_SELL         :NODE;
    CLKFF_SELH         :NODE;
    GEN_START_BIT      :NODE;
    GEN_STOP_BITFF     :DFF;
    STOP_SHIFT         :NODE;
    UNFREEZEFF         :DFFE;        % Unsynchronized UNFREEZE        %
    SNC_UNFREEZE       :DFF;         % Synchronized UNFREEZE          %
    DOUBLE_SNC         :DFF;         % Double Synchronized UNFREEZE   %
    FREEZEFF           :DFFE;        % Unsynchronized   FREEZE        %
    SNC_FREEZE         :DFF;         % Synchronized   FREEZE          %
    DOUBLE_FRZ         :DFF;         % Double Synchronized   FREEZE   %

BEGIN%*****%

% CHANDRA uses SIO's General Purpose Register Decode 0 -- Software sets    %
% to 800-8FF to enable the following decoded signals.                       %

GPCS0 = LCELL (!ECS[2] & ECS[1] & !ECS[0] & /ECSEN);

% Hard Disk Light I/O address range : 0808                                 %

 LIGHT_STRB = !A[7] & !A[6] & !A[5] & !A[4] & A[3] & !A[2]
            & !A[1] & !A[0] & GPCS0; HDD_LEDFF.s = XD[0] & LIGHT_STRB;
 HDD_LEDFF.r = !XD[0] & LIGHT_STRB;
 HDD_LEDFF.clk= GLOBAL(/XIOW);
 HDD_LEDFF.clrn=  (/RESET);
```

```
 /HDD_LED    = !HDD_LEDFF.q;
 %%
 % Equipment present Read Command 1 (I/O address range: 080C)           %
 %%
 /PRSNT_RD   = ! (!A[7] & !A[6] & !A[5] & !A[4] & A[3] & A[2]
                    & !A[1] & !A[0] & GPCS0 & !/XIOR);
 %%
 % Equipment present Read Command 2 (I/O address range: 080D)           %
 %%
 /L2_STATUS_RD = !(!A[7] & !A[6] & !A[5] & !A[4] & A[3] & A[2]
                        & !A[1] & A[0] & GPCS0 & !/XIOR);
 %%
 % External/Internal Planar ID I/O address range: 0852                    %
 %%
 /PLANAR_ID_RD  = !(!A[7] & A[6] & !A[5] & A[4] & !A[3] & !A[2]
                         & A[1] & !A[0] & GPCS0 & !/XIOR);
 %%
 % Keyboard Chip Select I/O address range = 0060, 0062, 0064, 0066–       %
 %%
 /KYBD_CS = !(!ECS[2] & ECS[1] & !ECS[0] & !/ECSEN);

 % Keyboard interupt (INT1) Clear = KBD_CS qualified with XIOR %

 CLRINT1 =!ECS[2] & ECS[1] & !ECS[0] & !/ECSEN & !/XIOR; INT1FF.d=VCC;
 INT1FF.clk = IRQ1;      % Set Keyboard INT1 latch on rising edge of IN1 %
 INT1FF.clrn = /RESET & !CLRINT1;
 IRQ1_OUT = INT1FF.q;

%%
% RTC_ALE I/O address 0070                                               %
%%
 RTC_ALE = (!A[2] & !A[1] & !A[0] & !ECS[2] & !ECS[1] & !/ECSEN & !/XIOW) ;
 %%

 % RTCWR I/O address 0071                                                 %
 %%
 /RTCWR = !(!A[2] & !A[1] &  A[0] & !ECS[2] & !ECS[1] & !/ECSEN & !/XIOW);
 %%

 % RTCDS I/O address 0071                                                 %
 %%
 /RTCDS = !(!A[2] & !A[1] &  A[0] & !ECS[2] & !ECS[1] & !/ECSEN & !/XIOR);
 %%

 % Nvram AS0 I/O address 0074                                             %
 %%
 /AS0   = !(A[2] & !A[1] & !A[0] & !ECS[2] & !ECS[1] & !/ECSEN & !/XIOW);
 %%

 % Nvram AS1 I/O address range: 0075                                      %
 %%
 /AS1   = !(A[2] & !A[1] &  A[0] & !ECS[2] & !ECS[1] & !/ECSEN & !/XIOW);
 %%

 % Nvram RTC WER I/O address 0077                                         %
 %%
```

```
 /NVRAMWE = !(A[2] &  A[1] &  A[0] & !ECS[2] & !ECS[1] & !/ECSEN & !/XIOW);
 %%

 % Nvram RTC OER I/O address range: 0077                                    %
 %%
 /NVRAMOE = !(A[2] &  A[1] &  A[0] & !ECS[2] & !ECS[1] & !/ECSEN & !/XIOR)
; %%

 % DRAM_PD_RD1 enables Present Detect I/O address range: 0880              %
 %%
  /DRAM_PD_RD1  =  !(A[7] & !A[6] & !A[5] & !A[4] & !A[3] & !A[2] & !A[1]
                    & !A[0] & GPCS0 & !/XIOR);
```

```
 %%
 % DRAM_PD_RD2 enables Present Detect I/O address range: 0881              %
 %%
  /DRAM_PD_RD2  =  !(A[7] & !A[6] & !A[5] & !A[4] & !A[3] & !A[2] & !A[1]
                  & A[0]  & GPCS0 & !/XIOR);

%%
%*************************************************************************%
%               POWER MANAGEMENT                                          %
%                                                                         %
%*************************************************************************%
% Write Power Control Register 1 I/O address: 082A                        %
%                                                                         %
% (MSB)     Bits 7–5   Reserved                                           %
%           Bit 4      I/O Strobe Key                        (W/O)        %
%           Bits 3–1   Data/Command B[3..1] to 83C750        (W/O)        %
% (LSB)     Bit 0      83C750 D0                             (R/W)        %
%*************************************************************************%

 83CX_CS =    (!A[7] & !A[6] & A[5] & !A[4] & A[3] & !A[2] & A[1] & GPCS0);
 PWR_REG1_STRB = 83CX_CS & !A0;

%%
% –Write ZERO to 83C750                                                   %
%%
 RWD0_STRB        = (PWR_REG1_STRB & !/XIOW & !XD[0]);
 RWD0             = TRI (GND, RWD0_STRB);

%%
% 83C750 I/O Strobe Key                                                   %
%%
/IO_STROBE        = !(XD[4] & PWR_REG1_STRB & !/XIOW & PROC_RDY
                   & !83CX_RESET);

%IO_CHRDY         = TRI (GND, IO_STRB);%

%*************************************************************************%
% Write Power Control Register 2 I/O address: 082B                        %
%                                                                         %
% (MSB)     Bit 7      CPU1 ROM Completed   (Reset by /RESET,    W/R)     %
%           Bit 6      Reserved                                           %
%           Bit 5      Reserved                                           %
%           Bit 4      Reserved                                           %
%           Bit 3      IRQ12 Mask           (Reset by /RESET)    (W/R)    %
%           Bits 2–1   Reserved                                           %
% (LSB)     Bit 0      Reset 83C750                          (W/O)    %
%*************************************************************************%
 PWR_REG2_STRB = 83CX_CS & A0;
 PWR_REG2[1].s     = XD[3] & PWR_REG2_STRB;
 PWR_REG2[1].r     = !XD[3] & PWR_REG2_STRB;
 PWR_REG2[1].clrn  =  (/RESET);
 PWR_REG2[2].s     = XD[7] & PWR_REG2_STRB;
 PWR_REG2[2].r     = !XD[7] & PWR_REG2_STRB;
 PWR_REG2[2].clrn  =  (/RESET);
 PWR_REG2[0].s     = XD[0] & PWR_REG2_STRB;
 PWR_REG2[0].r     = !XD[0] & PWR_REG2_STRB;
```

```
 PWR_REG2[0].clrn  = VCC;
 PWR_REG2[].clk    = GLOBAL(/XIOW);
 83CX_RESET        = PWR_REG2[0].q;
 IRQ12_MASK        = PWR_REG2[1].q;

%*************************************************************************%
% This output should be NORed with IRQ1 and EXTACTIV signals externally to%
% provide a real Activity Alert to the 87C350 (because of restriction of  %
% CHANDRA's IO pins.)                                                     %
%                                                                         %
%*********************%
 /ACTIVITY = !(IRQ1 # !IRQ12_MASK & IRQ12 # !/EXT_ACTVTY);


%*************************************************************************%
% Freeze Clock Logic – Refer to the Motorola MC88LV970 PLL Clock Driver   %
% Specification for information on Freeze Data protocol.                  %
%                                                                         %
% Freeze Clock Logic contains a 12 Bit serial shift register             %
% Decode the low order CLKFF[7..0] on addresses: 0860 –0861              %
% Decode the high order CLKFF[12..8] on addresses: 0862 –0863            %
%*************************************************************************%CL
KFF_STRB    = (!A[7] & A[6] & A[5] & !A[4] & !A[3] & !A[2] & GPCS0);
CLKFF_WR   = CLKFF_STRB & !/XIOW;
CLKFF_SELL = CLKFF_STRB & !A[1];
CLKFF_SELH = CLKFF_STRB & A[1];
CLKFF[12..0].prn  = VCC;
CLKFF[12..0].clrn = /RESET;
CLKFF[12..0].ena = START_SHIFTFF.q # CLKFF_WR;
CLKFF[12..0].clk  = ISA_CLK;

if START_SHIFTFF.q then                          % Shift with wraparound %
   CLKFF[11..0].d = CLKFF[12..1].q;
   CLKFF[12].d    = CLKFF[0].q;
else  if CLKFF_SELL then                         % Write to CLKFF[7..0]  %
   CLKFF[7..0].d  = XD[7..0];
   CLKFF[12..8].d = CLKFF[12..8].q;
      else if CLKFF_SELH then
             CLKFF[7..0].d = CLKFF[7..0].q;      % Write to CLKFF[12..8] %
             CLKFF[12..8].d = XD[4..0];
          else
             CLKFF[12..0].d = CLKFF[12..0].q;    % Do nothing            %
          end if;
      end if;
end if;

%*************************************************************************%
% UNFREEZE Flip Flop is cleared asynchronously when the UNFREEZE signal   %
% makes a low to high transition. It is set once shifting has been enabled%
% The CHANDRA ignores the UNFREEZE signal if the 601 PCLK clocks are not  %
% frozen.                                                                 %
%*************************************************************************%UN-
FREEZEFF.prn    = !SNC_SHIFT_ENFF.q & /RESET;
UNFREEZEFF.clrn = VCC;
UNFREEZEFF.ena  = !SHIFT_ENFF.q ;
UNFREEZEFF.d    = !(CLKFF[0].q # CLKFF[1].q);
```

```
UNFREEZEFF.clk  =  UNFREEZE ;

%************************************************************************%
% This signal is the UNFREEZE Flip Flop synchronized to the ISA clock.    %
%************************************************************************%
SNC_UNFREEZE.prn  = /RESET;
SNC_UNFREEZE.clrn = VCC;
SNC_UNFREEZE.d    = UNFREEZEFF.q;
SNC_UNFREEZE.clk  = ISA_CLK;

%************************************************************************
%
% This signal is the UNFREEZE Flip Flop double synchronized to the ISA
clock.%
%************************************************************************
%
DOUBLE_SNC.prn  = /RESET;
DOUBLE_SNC.clrn = VCC;
DOUBLE_SNC.d    = SNC_UNFREEZE.q;
DOUBLE_SNC.clk  = ISA_CLK;

%************************************************************************%
% FREEZE Flip Flop is cleared asynchronously when the UNFREEZE   signal   %
% makes a high to low transition. It is set once shifting has been enabled%
% The CHANDRA ignores the UNFREEZE signal if the 601 PCLK clocks are      %
% already frozen.                                                         %
%************************************************************************%
FREEZEFF.prn  = !SNC_SHIFT_ENFF.q & /RESET;
FREEZEFF.clrn = VCC;
FREEZEFF.ena  = !SHIFT_ENFF.q ;
FREEZEFF.d    = CLKFF[0].q & CLKFF[1].q;
FREEZEFF.clk  = !UNFREEZE ;

%************************************************************************%
% This signal is the FREEZE Flip Flop synchronized to the ISA clock.      %
%************************************************************************%
SNC_FREEZE.prn  = /RESET;
SNC_FREEZE.clrn = VCC;
SNC_FREEZE.d    = FREEZEFF.q;
SNC_FREEZE.clk  = ISA_CLK;

%************************************************************************
%
% This signal is the   FREEZE Flip Flop double synchronized to the ISA
clock.%
%************************************************************************
%
DOUBLE_FRZ.prn  = /RESET;
DOUBLE_FRZ.clrn = VCC;
DOUBLE_FRZ.d    = SNC_FREEZE.q;
DOUBLE_FRZ.clk  = ISA_CLK;
SHIFT_ENFF.s    = CLKFF_SELH;     % Start shifting upon write to 862       %
SHIFT_ENFF.r    = GND;
SHIFT_ENFF.prn  = DOUBLE_SNC.q & DOUBLE_FRZ;
SHIFT_ENFF.clrn = !GEN_STOP_BITFF.q & /RESET;  %Clr when it reaches 15 & rst%
SHIFT_ENFF.clk  = /XIOW;SNC_SHIFT_ENFF.d = SHIFT_ENFF.q;
```

```
                                                % One clock after SHIFT_ENFF%
SNC_SHIFT_ENFF.ena = /RESET;
SNC_SHIFT_ENFF.clrn = /RESET;
SNC_SHIFT_ENFF.clk = ISA_CLK;
CNTR[].clk  = ISA_CLK;
CNTR[].clrn = /RESET;              % Counter resets to zero                 %

If SNC_SHIFT_ENFF.q Then           % Count while SNC_SHIFT_ENFF is 1        %
   CNTR[].d = CNTR[].q + 1;
Else
   CNTR[].d = CNTR[].q;
End If;

GEN_START_BIT = !CNTR[3].q & !CNTR[2].q & !CNTR[1].q &  CNTR[0].q;  % 1 %
STOP_SHIFT    =  CNTR[3].q &  CNTR[2].q &  CNTR[1].q & !CNTR[0].q;  % 14 %
GEN_STOP_BITFF.d = STOP_SHIFT;  %Generate Stop Bit when counter is 15 %
GEN_STOP_BITFF.prn = VCC;
GEN_STOP_BITFF.clrn = /RESET;
GEN_STOP_BITFF.clk = ISA_CLK;
START_SHIFTFF.s    = GEN_START_BIT;
START_SHIFTFF.r    = STOP_SHIFT;
START_SHIFTFF.clrn = /RESET;
START_SHIFTFF.clk  = ISA_CLK;

%************************************************************************%
% FRZ_DATA_OUT is a 1 when the counter = 0.  It is also a 1 whenever     %
% START_SHIFTFF is 1 and CLKFF[0] is a 1 and then when the counter is    %
% Fifteen to leave it in the high state.                                 %
%************************************************************************%
FRZ_DATA_OUT =  !CNTR[3].q & !CNTR[2].q & !CNTR[1].q &  !CNTR[0].q
             # GEN_STOP_BITFF.q
             # START_SHIFTFF.q & !CLKFF[0].q;


%************************************************************************%
% Read Storage Light Status Register I/O address: 0808                   %
% (MSB)     Bits 7-1 Reserved                                            %
% (LSB)     Bit 0   Hard Disk Active Light                    (W/R)      %
%                                                                        %
% Read  Power Control Register 1 I/O address: 082A                       %
% (MSB)     Bits 7-1   Reserved                                          %
% (LSB)     Bit 0      83C750 D0                              (W/R)      %
%                                                                        %
% Read Power Control Register 2 I/O address: 082B                        %
% (MSB)     Bit 7      CPU1 ROM Completed   (Reset by /RESET,     R/W)    %
%           Bit 6      Reserved                                         %
%           Bit 5      Reserved                                         %
%           Bit 4      Reserved                                         %
%           Bit 3      IRQ12 Mask           (Reset by /RESET,     W/R)    %
%           Bits 2-1   Reserved                                         %
% (LSB)     Bit 0      83C750 Status                          (R/O)      %
%                                                                        %
%************************************************************************%
XD_TRI_OE  =  ((LIGHT_STRB
                  # PWR_REG1_STRB # PWR_REG2_STRB
                  # CLKFF_STRB) & !/XIOR);
```

```
XD[0]       = TRI (D[0], XD_TRI_OE);
D[0]        = HDD_LEDFF & LIGHT_STRB
               # RWD0 & PWR_REG1_STRB
               # PROC_RDY & /CMD_STATE & PWR_REG2_STRB
               # CLKFF[0].q & CLKFF_SELL
               # CLKFF[8].q & CLKFF_SELH;

XD[1]       = TRI (D[1], XD_TRI_OE);
D[1]        = CLKFF[1].q & CLKFF_SELL
               # CLKFF[9].q & CLKFF_SELH;
XD[2]       = TRI (D[2], XD_TRI_OE);
D[2]        = CLKFF[2].q & CLKFF_SELL
               # CLKFF[10].q & CLKFF_SELH;
XD[3]       = TRI (D[3], XD_TRI_OE);
D[3]        = PWR_REG2[1].q & PWR_REG2_STRB
               # CLKFF[3].q & CLKFF_SELL
               # CLKFF[11].q & CLKFF_SELH;
XD[4]       = TRI (D[4], XD_TRI_OE);
D[4]        = CLKFF[4].q & CLKFF_SELL
               # CLKFF[12].q & CLKFF_SELH;
XD[5]       = TRI (D[5], XD_TRI_OE);
D[5]        = CLKFF[5].q & CLKFF_SELL;
XD[6]       = TRI (D[6], XD_TRI_OE);
D[6]        = CLKFF[6].q & CLKFF_SELL;
XD[7]       = TRI (D[7], XD_TRI_OE);
D[7]        = PWR_REG2[2].q & PWR_REG2_STRB
               # CLKFF[7].q & CLKFF_SELL;
END;
```

Appendix C
Planar Set Up and Registers

This section describes the registers and setup considerations that are a function of the example planar, as opposed to the MCM. These settings and registers are not in general required by the MCM in every system. This information is included only for reference.

Designers of systems containing components similar to those found on the example planar may wish to start their development work using these settings.

C.1 ISA Bridge (SIO) Initialization

The example planar uses an Intel 82378ZB SIO as the ISA bridge.

The SIO chip must be configured prior to any other PCI bus agent. The SIO PCI arbiter is automatically enabled upon power-on reset. During power-on reset, the SIO drives the A/D(31:0), C/BE#(3:0), and par signals on the PCI bus.

The system I/O EPLD uses the decode circuits in the SIO that produce the signals ECSADDR[2:0] and UBUSCOE# to decode the motherboard register addresses. For this reason, utility bus A and B decode registers must be initialized as shown in Table C-1.

The ISA clock divisor must be set as indicated prior to running any CPU to PCI transactions. If the configuration information is stored in Flash, this should pose no problem.

The SIO must be programmed so that interval timer 1 operates in mode 2 with a period of approximately 15 microseconds. This timer controls the ISA refresh interval. It must be programmed at least 200 microseconds before any access to ISA DRAM is attempted.

PCI memory write cycles destined for ISA can use a 32-bit posted write buffer in the SIO. Bit 2 of the PCI control register controls the enabling of the posted write buffer. The default (power-on reset) state for the posted write buffer is disabled. It is required that the posted write buffer be enabled.

Note that PCI burst transactions are not supported by the SIO. For burst transactions, the SIO will always target abort after the first data phase. The system will not allow the CPU to burst to the SIO (or any other PCI agent). No PCI master should be programmed to attempt burst transactions to the SIO.

The SIO defaults (after power-on reset) to the slow sampling point (bits 4:3 of the PCI Control Register) for its subtractive decode. Of the three choices for the sampling point: slow (5 PCI cycles), typical (4 PCI cycles) and fast (3 PCI cycles), one should be chosen that is one clock after the slowest I/O device on the PCI bus. If the PCI agents are all memory mapped above 16M Byte and all I/O mapped above 64K, then the fast sampling point for

the subtractive decode can be chosen. This insures that no other PCI agent except the SIO will claim these addresses. Configure PCI agents in this manner to improve performance.

The SIO automatically inserts a 4 ISA clock cycle delay between PCI originated back-to-back 8 and 16 bit I/O cycles to the ISA bus. In addition, the ISA Controller Recovery Timer Register (configuration register, address offset=4Ch) enables a number of additional ISA clock cycles of delay to be inserted between these types of back-to-back I/O cycles. The ISA Controller Recovery Timer Register defaults (after power-on reset) to 2 additional ISA clock cycles of delay, making the total delay equal to 6 ISA clock cycles, for both the 8 and 16 bit I/O recovery times. Since none of the native I/O devices on the example planar require such long recovery times, the additional cycles specified by the ISA Controller Timer Register can be disabled. If an ISA card requiring a long recovery time is supported, the driver should insure that the recovery time is met.

Disable scatter/gather mode and GAT mode.

Do not attempt to access DMA channel 4 address and byte count registers.

Always enable the ISA master and DMA buffers. In order to isolate slow ISA Bus I/O devices from the PCI bus, the DMA controller uses the DMA/ISA master Line Buffer. This buffer can operate in single transaction or in 8-byte mode. Bits 0-LE/7-BE and 1-LE/6-BE of the PCI Control register configure the line buffer for DMA and ISA masters separately. It is required that the 8-byte mode be enabled for both (Bits = 1,1).

The registers in Table C-1 must be set in order for the example planar I/O hardware to operate properly. Vendors use LE bit nomenclature, and nomenclature within CPU registers is BE.

Table C-1. Summary of SIO Register Setup (Configuration Address = 8080 08xx)

Register	Addr	Bit	Set To	Reset Value	DESCRIPTION
PCI Control Register	40h	2-LE 5-BE	1	0	Enable PCI Memory Posted Write Buffer.
PCI Control Register	40h	1-LE 6-BE	1	0	Enable ISA Master Line buffer.
PCI Control Register	40h	0-LE 7-BE	1	0	Enable DMA Line Buffer
PCI Arbiter Control (Config/PCI)	41h	0-LE 7-BE	0	0	Disable GAT (Guaranteed Access Time Mode). Note: GAT does not work in SIO.
ISA Clock Divisor (Config/PCI)	4Dh	5-LE 2-BE	0	0	Disable Coprocessor Error Support.
ISA Clock Divisor (Config/PCI)	4Dh	4-LE 3-BE	1	0	Enable IRQ12/M Mouse Support.
ISA Clock Divisor (Config/PCI)	4Dh	3-LE 4-BE	*	0	* This bit should be set to 1 before changing or loading the PCI ISA Clock Divisor value. Setting this bit to 1 will assert the RSTDVR signal (which resets the System I/O EPLD and any devices on the ISA bus slots). All these devices will require reconfiguration after this bit has been asserted. Software must guarantee that RSTDVR be asserted for a minimum of 1 ms after the clock divisor value is set.
ISA Clock Divisor (Config/PCI)	4Dh	2:0-LE 5:7-BE	*	0	* Set this field to 000b (divisor = 4). (If PCI clock is slower than 33 MHz, then this field would be 001b (divisor=3).

Table C-1. Summary of SIO Register Setup (Configuration Address = 8080 08xx) (Continued)

Register	Addr	Bit	Set To	Reset Value	DESCRIPTION
Utility Bus Chip Select A (Config/PCI)	4Eh	4-LE 4-BE	1	0	Disable generation of ECSADDR(2:0) and UBUSOE# for the IDE and Floppy decode.
Utility Bus Chip Select A (Config/PCI)	4Eh	1-LE 6-BE	1	1	Enable keyboard addresses (60h, 62h, 64h, 66h).
Utility Bus Chip Select A (Config/PCI)	4Eh	0-LE 7-BE	1	1	Enable TOD Addresses (70h, 71h).
Utility Bus Chip Select B (Config/PCI)	4Fh	7-LE 0-BE	1	0	Enable access to the motherboard registers in the 0800-08FF address range.
Utility Bus Chip Select B (Config/PCI)	4Fh	6-LE 1-BE	1	1	Enable Port 92h access.
Utility Bus Chip Select B (Config/PCI)	4Fh	5:4-LE 2:3-BE	11	00	Disable generation of default address for Parallel Port.
Utility Bus Chip Select B (Config/PCI)	4Fh	3:2-LE 4:5-BE	11	00	Disable generation of default address for Serial Port B.
Utility Bus Chip Select B (Config/PCI)	4Fh	1:0-LE 6:7-BE	11	00	Disable generation of default address for Serial Port A.
Interrupt Controller 1 - ICW1 (I/O /PCI)	20h	3-LE 4-BE	0	x	Set Interrupt Controller 1 to edge triggered mode.
Interrupt Controller 1 - ICW1 (I/O /PCI)	20h	1-LE 6-BE	0	x	Set Interrupt Controller 1 to cascade mode.
Interrupt Controller 2 - ICW1 (I/O /PCI)	A0h	3-LE 4-BE	0	x	Set Interrupt Controller 2 to edge triggered mode.
Interrupt Controller 2 - ICW1 (I/O /PCI)	A0h	1-LE 6-BE	0	x	Set Interrupt Controller 2 to cascade mode.
NMI Status and Control (I/O / PCI)	61h	3-LE 4-BE	0	0	IOCHK# NMI enabled.
NMI Status and Control (I/O / PCI)	61h	2-LE 5-BE	0	0	PCI SERR# NMI enabled.
NMI Enable and TOD Address (I/O /PCI)	70h	7-LE 0-BE	0	1	NMI interrupt enabled.
DMA Command (I/O /PCI)	08h, D0h	7-LE 0-BE	0	0	DACK# Assert Level set to low.
DMA Command (I/O /PCI)	08h, D0h	6-LE 1-BE	0	0	DREQ Sense Level set to high.

C.1.1 Summary of SIO Configuration Registers

Table C-2. Summary of SIO Configuration Registers

Address	Description	Type	Reset Value	Set To *
8080 0800	Vendor Identification	R/O	86h	
8080 0801	Vendor Identification	R/O	80	
8080 0802	Device Identification	R/O	84	
8080 0803	Device Identification	R/O	04	
8080 0804	Command	R/W	07	0F
8080 0805	Command	R/W	00	00
8080 0806	Device Status	R/W	00	
8080 0807	Device Status	R/W	02	
8080 0808	Revision Identification	R/W	00	
8080 0840	PCI Control	R/W	20	21
8080 0841	PCI Arbiter Control	R/W	00	00
8080 0842	PCI Arbiter Priority Control	R/W	04	04
8080 0843	PCI Arbiter Priority Control Extension	R/W	00	00
8080 0844	MEMCS# Control	R/W	00	00
8080 0845	MEMCS# Bottom of Hole	R/W	10	10
8080 0846	MEMCS# Top of Hole	R/W	0F	0F
8080 0847	MEMCS# Top of Memory	R/W	00	00
8080 0848	ISA Address Decoder Control	R/W	01	F1
8080 0849	ISA Address Decoder ROM Block	R/W	00	00
8080 084A	ISA Address Bottom of Hole	R/W	10	10
8080 084B	ISA Address Top of Hole	R/W	0F	0F
8080 084C	ISA Controller Recovery Timer	R/W	56	56
8080 084D	ISA Clock Divisor	R/W	40	10
8080 084E	Utility Bus Chip Select A	R/W	07	07
8080 084F	Utility Bus Chip Select B	R/W	4F	FF
8080 0854	MEMCS# Attribute Register #1	R/W	00	
8080 0855	MEMCS# Attribute Register #2	R/W	00	
8080 0856	MEMCS# Attribute Register #3	R/W	00	
8080 0857	Scatter/Gather Relocation Base	R/W	04	
8080 0860	PIRQ Route Control 0	R/W	80	0F
8080 0861	PIRQ Route Control 1	R/W	80	0F
8080 0862	PIRQ Route Control 2	R/W	80	80
8080 0863	PIRQ Route Control 3 (unused)	R/W	80	80
8080 0880	BIOS Timer Base Address	R/W	78	
8080 0881	BIOS Timer Base Address	R/W	00	

Note: * If the entry in this column is blank, then the boot firmware does not write to this register.

C.2 Example Planar Combined Register Listing

C.2.1 Direct Access Registers

Table C-3 contains a summary listing of the registers that are physically located on the example planar. These registers are generally accessed using single CPU transfers. There is an additional set of registers (see Table 9-2) located in the 660 bridge, which are accessed using pairs of CPU transfers.

Table C-3. Combined Register Listing

ISA Port	Contiguous Mode Addr	Non-Contig Mode Addr	Description	R/W	Set To (6)	Loc (4)	Note
0000	8000 0000	8000 0000	DMA1 CH0 Base and Current Addr	R/W	—	SIO	
0001	8000 0001	8000 0001	DMA1 CH0 Base and Current Cnt	R/W	—	SIO	
0002	8000 0002	8000 0002	DMA1 CH1 Base and Current Addr	R/W	—	SIO	
0003	8000 0003	8000 0003	DMA1 CH0 Base and Current Cnt	R/W	—	SIO	
0004	8000 0004	8000 0004	DMA1 CH2 Base and Current Addr	R/W	—	SIO	
0005	8000 0005	8000 0005	DMA1 CH2 Base and Current Cnt	R/W	—	SIO	
0006	8000 0006	8000 0006	DMA1 CH3 Base and Current Addr	R/W	—	SIO	
0007	8000 0007	8000 0007	DMA1 CH3 Base and Current Cnt	R/W	—	SIO	
0008	8000 0008	8000 0008	DMA1 Status(R) Command(W)	R/W	—	SIO	
0009	8000 0009	8000 0009	DMA1 Soft Request	W	—	SIO	
000A	8000 000A	8000 000A	DMA1 Write Single Mask Bit	W	—	SIO	
000B	8000 000B	8000 000B	DMA1 Write Mode	W	—	SIO	
000C	8000 000C	8000 000C	DMA1 Clear Byte Pointer	W	—	SIO	
000D	8000 000D	8000 000D	DMA1 Master Clear	W	—	SIO	
000E	8000 000E	8000 000E	DMA1 Clear Mask	W	—	SIO	
000F	8000 000F	8000 000F	DMA1 R/W All Mask Register Bits	R/W	—	SIO	
0020	8000 0020	8000 1000	INT1 Control	R/W	—	SIO	
0021	8000 0021	8000 1001	INT1 Mask	R/W	—	SIO	
0040	8000 0040	8000 2000	Timer Counter 1 - Counter 0 Cnt	R/W	—	SIO	
0041	8000 0041	8000 2001	Timer Counter 1 - Counter 1 Cnt	R/W	—	SIO	
0042	8000 0042	8000 2002	Timer Counter 1 - Counter 2 Cnt	R/W	—	SIO	
0043	8000 0043	8000 2003	Timer Counter 1 Command Mode	W	—	SIO	
0060	8000 0060	8000 3000	Reset X-Bus (mse) IRQ12 and Kbd	R	—	SIO	
0061	8000 0061	8000 3001	NMI Status and Control	R/W	—	SIO	
0062	8000 0062	8000 3002	Reserved for Keyboard/Mouse	R/W	—	KBD	(3)
0064	8000 0064	8000 3004	Keyboard/Mouse	R	—	KBD	(3)
0066	8000 0066	8000 3006	Reserved for Keyboard/Mouse	R/W	—	KBD	(3)
0070	8000 0070	8000 3010	TOD Addr and NMI Enable	W	—	SIO	
0071	8000 0071	8000 3011	TOD Read/Write	R/W	—	RTC	(3)
0074	8000 0074	8000 3014	NV RAM Addr Strobe 0	W	—	NVR	(3)
0075	8000 0075	8000 3015	NV RAM Addr Strobe 1	W	—	NVR	(3)
0077	8000 0077	8000 3017	NV RAM Data Port	R/W	—	NVR	(3)
0078	8000 0078	8000 3018	BIOS Timer	R/W	—	SIO	
0079	8000 0079	8000 3019	BIOS Timer	R/W	—	SIO	
007A	8000 007A	8000 301A	BIOS Timer	R/W	—	SIO	
007B	8000 007B	8000 301B	BIOS Timer	R/W	—	SIO	
0080	8000 0080	8000 4000	DMA Page Register Reserved	R/W	—	SIO	
0081	8000 0081	8000 4001	DMA Channel 2 Page Register	R/W	—	SIO	
0082	8000 0082	8000 4002	DMA Channel 3 Page Register	R/W	—	SIO	
0083	8000 0083	8000 4003	DMA Channel 1 Page Register	R/W	—	SIO	
0084	8000 0084	8000 4004	DMA Page Register Reserved	R/W	—	SIO	
0085	8000 0085	8000 4005	DMA Page Register Reserved	R/W	—	SIO	
0086	8000 0086	8000 4006	DMA Page Register Reserved	R/W	—	SIO	
0087	8000 0087	8000 4007	DMA Channel 0 Page Register	R/W	—	SIO	
0088	8000 0088	8000 4008	DMA Page Register Reserved	R/W	—	SIO	

Table C-3. Combined Register Listing (Continued)

ISA Port	Contiguous Mode Addr	Non-Contig Mode Addr	Description	R/W	Set To (6)	Loc (4)	Note
0089	8000 0089	8000 4009	DMA Channel 6 Page Register	R/W	—	SIO	
008A	8000 008A	8000 400A	DMA Channel 7 Page Register	R/W	—	SIO	
008B	8000 008B	8000 400B	DMA Channel 5 Page Register	R/W	—	SIO	
008C	8000 008C	8000 400C	DMA Page Register Reserved	R/W	—	SIO	
008D	8000 008D	8000 400D	DMA Page Register Reserved	R/W	—	SIO	
008E	8000 008E	8000 400E	DMA Page Register Reserved	R/W	—	SIO	
008F	8000 008F	8000 400F	DMA Low Page Register Refresh	R/W	—	SIO	
0090	8000 0090	8000 4010	DMA Page Register Reserved	R/W	—	SIO	
0092	8000 0092	8000 4012	Special Port 92 Register	R/W	—	660	
0094	8000 0094	8000 4014	DMA Page Register Reserved	R/W	—	SIO	(2)
0095	8000 0095	8000 4015	DMA Page Register Reserved	R/W	—	SIO	
0096	8000 0096	8000 4016	DMA Page Register Reserved	R/W	—	SIO	
0098	8000 0098	8000 4018	DMA Page Register Reserved	R/W	—	SIO	
009C	8000 009C	8000 401C	DMA Page Register Reserved	R/W	—	SIO	
009D	8000 009D	8000 401D	DMA Page Register Reserved	R/W	—	SIO	
009E	8000 009E	8000 401E	DMA Page Register Reserved	R/W	—	SIO	
009F	8000 009F	8000 401F	DMA Low Page Register Refresh	R/W	—	SIO	
00A0	8000 00A0	8000 5000	INT2 Control Register	R/W	—	SIO	
00A1	8000 00A1	8000 5001	INT2 Mask Register	R/W	—	SIO	
00C0	8000 00C0	8000 6000	DMA2 CH0 Base and Current Addr	R/W	—	SIO	
00C2	8000 00C2	8000 6002	DMA2 CH0 Base and Current Cnt	R/W	—	SIO	
00C4	8000 00C4	8000 6004	DMA2 CH1 Base and Current Addr	R/W	—	SIO	
00C6	8000 00C6	8000 6006	DMA2 CH1 Base and Current Cnt	R/W	—	SIO	
00C8	8000 00C8	8000 6008	DMA2 CH2 Base and Current Addr	R/W	—	SIO	
00CA	8000 00CA	8000 600A	DMA2 CH2 Base and Current Cnt	R/W	—	SIO	
00CC	8000 00CC	8000 600C	DMA2 CH3 Base and Current Addr	R/W	—	SIO	
00CE	8000 00CE	8000 600E	DMA2 CH3 Base and Current Cnt	R/W	—	SIO	
00D0	8000 000D	8000 6010	DMA2 Status(R) Command(W)	R/W	—	SIO	
00D2	8000 00D2	8000 6012	DMA2 Soft Request	W	—	SIO	
00D4	8000 00D4	8000 6014	DMA2 Write Single Mask Bit	W	—	SIO	
00D6	8000 00D6	8000 6016	DMA2 Write Mode	W	—	SIO	
00D8	8000 00D8	8000 6018	DMA2 Clear Byte Pointer	W	—	SIO	
00DA	8000 00DA	8000 601A	DMA2 Master Clear	W	—	SIO	
00DC	8000 00DC	8000 601C	DMA2 Clear Mask	W	—	SIO	
00DE	8000 00DE	8000 601E	DMA2 R/W All Mask Register Bits	R/W	—	SIO	
00F0	8000 00F0	8000 7010	Coprocessor Error Reg - Reserved	R/W	—	SIO	
040B	8000 040B	8002 0006	DMA1 Extended Mode	W	—	SIO	
0410	8000 0410	8002 0010	CH0 Scatter/Gather Command	W	—	SIO	
0411	8000 0411	8002 0011	CH1 Scatter/Gather Command	W	—	SIO	
0412	8000 0412	8002 0012	CH2 Scatter/Gather Command	W	—	SIO	
0413	8000 0413	8002 0013	CH3 Scatter/Gather Command	W	—	SIO	
0415	8000 0415	8002 0015	CH5 Scatter/Gather Command	W	—	SIO	
0416	8000 0416	8002 0016	CH6 Scatter/Gather Command	W	—	SIO	
0417	8000 0417	8002 0017	CH7 Scatter/Gather Command	W	—	SIO	
0418	8000 0418	8002 0018	CH0 Scatter/Gather Status	R	—	SIO	

Table C-3. Combined Register Listing (Continued)

ISA Port	Contiguous Mode Addr	Non-Contig Mode Addr	Description	R/W	Set To (6)	Loc (4)	Note
0419	8000 0419	8002 0019	CH1 Scatter/Gather Status	R	—	SIO	
041A	8000 041A	8002 001A	CH2 Scatter/Gather Status	R	—	SIO	
041B	8000 041B	8002 001B	CH3 Scatter/Gather Status	R	—	SIO	
041D	8000 041D	8002 001D	CH5 Scatter/Gather Status	R	—	SIO	
041E	8000 041E	8002 001E	CH6 Scatter/Gather Status	R	—	SIO	
041F	8000 041F	8002 001F	CH7 Scatter/Gather Status	R	—	SIO	
0420	8000 0420	8002 1000	CH0 Scatter/Gather Pointer	R/W	—	SIO	
0421	8000 0421	8002 1001	CH0 Scatter/Gather Pointer	R/W	—	SIO	
0422	8000 0422	8002 1002	CH0 Scatter/Gather Pointer	R/W	—	SIO	
0423	8000 0423	8002 1003	CH0 Scatter/Gather Pointer	R/W	—	SIO	
0424	8000 0424	8002 1004	CH1 Scatter/Gather Pointer	R/W	—	SIO	
0425	8000 0425	8002 1005	CH1 Scatter/Gather Pointer	R/W	—	SIO	
0426	8000 0426	8002 1006	CH1 Scatter/Gather Pointer	R/W	—	SIO	
0427	8000 0427	8002 1007	CH1 Scatter/Gather Pointer	R/W	—	SIO	
0428	8000 0428	8002 1008	CH2 Scatter/Gather Pointer	R/W	—	SIO	
0429	8000 0429	8002 1009	CH2 Scatter/Gather Pointer	R/W	—	SIO	
042A	8000 042A	8002 100A	CH2 Scatter/Gather Pointer	R/W	—	SIO	
042B	8000 042B	8002 100B	CH2 Scatter/Gather Pointer	R/W	—	SIO	
042C	8000 042C	8002 100C	CH3 Scatter/Gather Pointer	R/W	—	SIO	
042D	8000 042D	8002 100D	CH3 Scatter/Gather Pointer	R/W	—	SIO	
042E	8000 042E	8002 100E	CH3 Scatter/Gather Pointer	R/W	—	SIO	
042F	8000 042F	8002 100F	CH3 Scatter/Gather Pointer	R/W	—	SIO	
0434	8000 0434	8002 1014	CH5 Scatter/Gather Pointer	R/W	—	SIO	
0435	8000 0435	8002 1015	CH5 Scatter/Gather Pointer	R/W	—	SIO	
0436	8000 0436	8002 1016	CH5 Scatter/Gather Pointer	R/W	—	SIO	
0437	8000 0437	8002 1017	CH5 Scatter/Gather Pointer	R/W	—	SIO	
0438	8000 0438	8002 1018	CH6 Scatter/Gather Pointer	R/W	—	SIO	
0439	8000 0439	8002 1019	CH6 Scatter/Gather Pointer	R/W	—	SIO	
043A	8000 043A	8002 101A	CH6 Scatter/Gather Pointer	R/W	—	SIO	
043B	8000 043B	8002 101B	CH6 Scatter/Gather Pointer	R/W	—	SIO	
043C	8000 043C	8002 101C	CH7 Scatter/Gather Pointer	R/W	—	SIO	
043D	8000 043D	8002 101D	CH7 Scatter/Gather Pointer	R/W	—	SIO	
043E	8000 043E	8002 101E	CH7 Scatter/Gather Pointer	R/W	—	SIO	
043F	8000 043F	8002 101F	CH7 Scatter/Gather Pointer	R/W	—	SIO	
0481	8000 0481	8002 4001	DMA CH2 High Page	R/W	—	SIO	
0482	8000 0482	8002 4002	DMA CH3 High Page	R/W	—	SIO	
0483	8000 0483	8002 4003	DMA CH1 High Page	R/W	—	SIO	
0487	8000 0487	8002 4007	DMA CH0 High Page	R/W	—	SIO	
0489	8000 0489	8002 4009	DMA CH6 High Page	R/W	—	SIO	
048A	8000 048A	8002 400A	DMA CH7 High Page	R/W	—	SIO	
048B	8000 048B	8002 400B	DMA CH5 High Page	R/W	—	SIO	
04D0	8000 04D0	8002 6010	Interrupt Control 1	R/W	—	SIO	
04D1	8000 04D1	8002 6011	Interrupt Control 2	R/W	—	SIO	
04D6	8000 04D6	8002 6016	DMA2 Extended Mode	W	—	SIO	
0808	8000 0808	8004 0008	HDD Light	R/W	—	EPLD	

Table C-3. Combined Register Listing (Continued)

ISA Port	Contiguous Mode Addr	Non-Contig Mode Addr	Description	R/W	Set To (6)	Loc (4)	Note
080C	8000 080C	8004 000C	Equipment Present	R	—	logic	(3)
080D	8000 080D	8004 000D	L2 Cache Status Reg	R	—	logic	(3)
0814	8000 0814	8004 0014	L2 Flush	W	—	660	
081C	8000 081C	8004 001C	System Control 81C	R/W	(7)	660	
0821	8000 0821	8004 1001	Memory Controller Misc	R/W	—	660	
082A	8000 082A	8004 100A	Power Mgmt Control Reg1	R/W	—	EPLD	(5)
082B	8000 082B	8004 100B	Power Mgmt Control Reg2	R/W	—	EPLD	(5)
0840	8000 0840	8004 2000	Memory Parity Error Status	R	—	660	
0842	8000 0842	8004 2002	L2 Error Status	R	—	660	
0843	8000 0843	8004 2003	L2 Parity Read & Clear	R	—	660	
0844	8000 0844	8004 2004	Unsupported Transfer Type Error	R	—	660	
0850	8000 0850	8004 2010	I/O Map Type	W	—	660	
0852	8000 0852	8004 2012	Board ID	R	—	logic	(3)
0860	8000 0860	8004 3000	Freeze Clock Reg Low	R/W	—	EPLD	(3)
0862	8000 0862	8004 3002	Freeze Clock Reg High	R/W	—	EPLD	(3)
0880	8000 0880	8004 4000	SIMM Presence Detect Slot 1/2	R	—	logic	(3)
0881	8000 0881	8004 4001	SIMM Presence Detect Slot 3/4	R	—	logic	(3)
	8000 0CF8		PCI/BCR Configuration Address	R/W	—	660	
	8000 0CFC		PCI/BCR Configuration Data	R/W	—	660	
	8080 08xx		PCI Type 0 Configuration Addr	R/W	—	660	
	8080 0800		Vendor Identification	R	—	SIO	
	8080 0801		Vendor Identification	R	—	SIO	
	8080 0802		Device Identification	R	—	SIO	
	8080 0803		Device Identification	R	—	SIO	
	8080 0804		Command	R/W	0F	SIO	
	8080 0805		Command	R/W	00	SIO	
	8080 0806		Device Status	R/W	—	SIO	
	8080 0807		Device Status	R/W	—	SIO	
	8080 0808		Revision Identification	R/W	—	SIO	
	8080 0840		PCI Control	R/W	21	SIO	
	8080 0841		PCI Arbiter Control	R/W	00	SIO	
	8080 0842		PCI Arbiter Priority Control	R/W	04	SIO	
	8080 0843		PCI Arbiter Priority Control Extension	R/W	00	SIO	
	8080 0844		MEMCS# Control	R/W	00	SIO	
	8080 0845		MEMCS# Bottom of Hole	R/W	10	SIO	
	8080 0846		MEMCS# Top of Hole	R/W	0F	SIO	
	8080 0847		MEMCS# Top of Memory	R/W	00	SIO	
	8080 0848		ISA Address Decoder Control	R/W	F1	SIO	
	8080 0849		ISA Address Decoder ROM Block	R/W	00	SIO	
	8080 084A		ISA Address Bottom of Hole	R/W	10	SIO	
	8080 084B		ISA Address Top of Hole	R/W	0F	SIO	
	8080 084C		ISA Controller Recovery Timer	R/W	56	SIO	
	8080 084D		ISA Clock Divisor	R/W	10	SIO	
	8080 084E		Utility Bus Chip Select A	R/W	07	SIO	
	8080 084F		Utility Bus Chip Select B	R/W	FF	SIO	

Table C-3. Combined Register Listing (Continued)

ISA Port	Contiguous Mode Addr	Non-Contig Mode Addr	Description	R/W	Set To (6)	Loc (4)	Note
	8080 0854		MEMCS# Attribute Register #1	R/W	—	SIO	
	8080 0855		MEMCS# Attribute Register #2	R/W	—	SIO	
	8080 0856		MEMCS# Attribute Register #3	R/W	—	SIO	
	8080 0857		Scatter/Gather Relocation Base	R/W	—	SIO	
	8080 0860		PIRQ Route Control 0	R/W	0F	SIO	
	8080 0861		PIRQ Route Control 1	R/W	0F	SIO	
	8080 0862		PIRQ Route Control 2	R/W	80	SIO	
	8080 0863		PIRQ Route Control 3 (unused)	R/W	80	SIO	
	8080 0880		BIOS Timer Base Address	R/W	—	SIO	
	8080 0881		BIOS Timer Base Address	R/W	—	SIO	
	8080 10xx		PCI Type 0 Configuration Addr	R/W	—	660	
	8080 20xx		PCI Type 0 Configuration Addr	R/W	—	660	
	8080 40xx		PCI Type 0 Configuration Addr	R/W	—	660	
	8080 80xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	8081 00xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	8082 00xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	8084 00xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	8088 00xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	8090 00xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	80A0 00xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	80C0 00xx		PCI Type 0 Configuration Addr	R/W	—	660	(5)
	BFFF EFF0	BFFF EFF0	System Error Addr	R	—	660	(5)
	BFFF FFF0	BFFF FFF0	Interrupt Vector	R	—	660	
	FFFF FFF0	FFFF FFF0	Flash Write Addr/Data	W	—	660	
	FFFF FFF1	FFFF FFF1	Flash Lock Out	W	—	660	

Notes:

1. The first 5 hex digits in the contiguous and non-contiguous mode columns represent the memory page number for which the protection attributes may be set in contiguous I/O mode. That is, devices having the same first five digits in this column will have the same attributes in the memory page table.
2. Port 94 may be used by certain video controllers (e.g. Weitek™ 9100). The SIO chip positively decodes this port. Therefore bus contention may arise when both devices claim the PCI cycle to this port address. Bus contention results in invalid data and possibly harm to the hardware.
3. The control signals for these ports are partially decoded by the SIO. The System I/O EPLD completes the decodes, and issues control signals to the registers, which are usually X-bus buffers.
4. KBD = Keyboard / Mouse Controller
   RTC = Real Time Clock, also known as the TOD (Time Of Day clock)
   NVR = Non-Volatile RAM, in the same package as the RTC
   660 = The 660 Bridge.
5. Not used.
6. In the Set To column, a long dash — means that the initialization firmware does not write to this register. The register is either not used, not written to, or the value of it depends on changing circumstances.
   If the word Memory appears, please refer to the System Memory section of the 660 User's Manual.
7. Set register 81C to C0h if an L2 is installed, else leave at reset value.

C.3 ISA Bus Register Suggestions

The following port assignments are designed to be compatible with the example planar firmware and Super I/O type chips. These registers and functions are not implemented on the example planar motherboard.

Table C-4. Compatible ISA Ports (Not on Reference Board)

ISA Port	Contiguous Mode Addr	Non-Contig Mode Addr	Description	Note	R/W
01F0	8000 01F0	8000 F010	IDE Data		R/W
01F1	8000 01F1	8000 F011	IDE Error/Features		R/W
01F2	8000 01F2	8000 F012	IDE Sector Count		R/W
01F3	8000 01F3	8000 F013	IDE Sector Number		R/W
01F4	8000 01F4	8000 F014	IDE Cylinder Low		R/W
01F5	8000 01F5	8000 F015	IDE Cylinder High		R/W
01F6	8000 01F6	8000 F016	IDE Drive Head		R/W
01F7	8000 01F7	8000 F017	IDE Status/Command		R/W
0278	8000 0278	8001 3018	Parallel Port 2	(1)	R/W
0279	8000 0279	8001 3019	Parallel Port 2		R/W
027A	8000 027A	8001 301A	Parallel Port 2		R/W
027B	8000 027B	8001 301B	Parallel Port 2		R/W
027C	8000 027C	8001 301C	Parallel Port 2		R/W
027D	8000 027D	8001 301D	Parallel Port 2		R/W
02F8	8000 02F8	8001 7018	Serial Port 2		R/W
02F9	8000 02F9	8001 7019	Serial Port 2		R/W
02FA	8000 02FA	8001 701A	Serial Port 2		R/W
02FB	8000 02FB	8001 701B	Serial Port 2		R/W
02FC	8000 02FC	8001 701C	Serial Port 2		R/W
02FD	8000 02FD	8001 701D	Serial Port 2		R/W
02FE	8000 02FE	8001 701E	Serial Port 2		R/W
02FF	8000 02FF	8001 701F	Serial Port 2		R/W
0370	8000 0370	8001 B010	Secondary Floppy Digital Output		W
0371	8000 0371	8001 B011	Secondary Floppy Digital Output		W
0372	8000 0372	8001 B012	Secondary Floppy Digital Output		W
0373	8000 0373	8001 B013	Secondary Floppy Digital Output		W
0374	8000 0374	8001 B014	Secondary Floppy Digital Output		W
0375	8000 0375	8001 B015	Secondary Floppy Digital Output		W
0376	8000 0376	8001 B016	Secondary Floppy Digital Output		W
0377	8000 0377	8001 B017	Secondary Floppy Digital Output		W
0376	8000 0376	8001 B016	Secondary IDE Alt Status/Device Ctl		R/W
0377	8000 0377	8001 B017	Secondary IDE drive address		W
0378	8000 0378	8001 B018	Parallel Port 1	(1)	W
0379	8000 0379	8001 B019	Parallel Port 1		W
037A	8000 037A	8001 B01A	Parallel Port 1		W
037B	8000 037B	8001 B01B	Parallel Port 1		W
037C	8000 037C	8001 B01C	Parallel Port 1		W
037D	8000 037D	8001 B01D	Parallel Port 1		W
0398	8000 0398	8001 C018	Super I/O Index Address		R/W
0399	8000 0399	8001 C019	Super I/O Data Address		R/W
03BC	8000 03BC	8001 D01C	Parallel Port 3		R/W
03BD	8000 03BD	8001 D01D	Parallel Port 3		R/W
03BE	8000 03BE	8001 D01E	Parallel Port 3		R/W
03F0	8000 03F0	8001 F010	Primary Floppy Digital Output (Media Sense)		W/O
03F1	8000 03F1	8001 F011	Primary Floppy Digital Output		W/O

Table C-4. Compatible ISA Ports (Not on Reference Board) (Continued)

ISA Port	Contiguous Mode Addr	Non-Contig Mode Addr	Description	Note	R/W
03F2	8000 03F2	8001 F012	Primary Floppy Digital Output		W
03F3	8000 03F3	8001 F013	Primary Floppy Digital Output (Also Media Sense)		W
03F4	8000 03F4	8001 F014	Primary Floppy Digital Output		W
03F5	8000 03F5	8001 F015	Primary Floppy Digital Output		W
03F6	8000 03F6	8001 F016	Primary Floppy Digital Output		W
03F7	8000 03F7	8001 F017	Primary Floppy Digital Output		W
03F6	8000 03F6	8001 F016	Primary IDE Alt Status/Device Ctl		R/W
03F7	8000 03F7	8001 F017	Primary IDE Drive Address		R
03F8	8000 03F8	8001 F018	Serial Port 1		R/W
03FA	8000 03FA	8001 F01A	Serial Port 1		R/W
03FB	8000 03FB	8001 F01B	Serial Port 1		R/W
03FC	8000 03FC	8001 F01C	Serial Port 1		R/W
03FD	8000 03FD	8001 F01D	Serial Port 1		R/W
03FE	8000 03FE	8001 F01E	Serial Port 1		R/W
03FF	8000 03FF	8001 F01F	Serial Port 1		R/W

Note:
1. This is a preferred location for this function.

Appendix D
Planar Electromechanical

D.1 Electrical

D.1.1 Power Requirements

This section sets out the power supply requirements for the example planar. They are achievable with low-cost PC power supplies (see Table D-1 for specifications and Table D-2 for approximate power consumption).

Table D-1. Power Supply Specification

Output	Tolerance	Maximum Ripple P–P
+5V	+5% –4%	50 mV
+12V	+5% –5%	120 mV
–12V	+10% –9%	120 mV
–5V* (1)	+10% –10%	120 mV
3.3V (2)	+5% –4%	50 mV

Table D-2. Approximate Power Consumption

Element	+5V (Amp)	+12V (Amp)	–12V (Amp)	–5V (Amp) (1)	3.3V (Amp) (2)
Base motherboard with 1 8M SIMM running typical code	3.0	0.1	0.02	0	0
8M DRAM standby/refresh (each)	0.18	0	0	0	0
32M DRAM standby/refresh (each)	0.16	0	0	0	0
256K SRAM L2 Cache	1.6	0	0	0	0
Each PCI Slot – allocation (3)	3.0 max	0.3 max	0.06 max	0	3.3 max
Each ISA Slot – allocation (3)(4)	4.5 max	1.5 max	0.3 max	0.2 max	0
Main Power Connector Capacity (at 5.0 amp./pin—20 amp. DC return)	20.0	5.0	5.0	0.5	0

Notes for Table D-1 and Table D-2:

1. The –5v is not used on the planer, but it is routed from the power supply connector to the ISA slots.
2. The 3.3v to the PCI bus slots comes from the power supply connector. The 3.3v for the CPU and the 660 bridge is a separate supply, generated from the +5v supply by a linear regulator.
3. These power requirements are allocated by the system designer. The currents specified per slot are also the maximum currents which may be consumed by the bus. Because of this, the total currents for all the cards used for either the PCI slot or the ISA slot must not exceed the amounts listed for those slots.
4. ISA slot information is taken from IEEE P996.

Other requirements are:

1. Overshoot on any supply voltage must be less than 10% of nominal and must decay to within the regulation band within 50 msec.
2. In any failure situation, the power supply must shut down before the +5v output reaches 6.5V to give the motherboard a reasonable chance of surviving; however, damage may occur at any voltage above 5.5V.
3. Power_Good Signal Requirements
   - The signal must be at a TTL down level when power is applied until >100 msec to 500 msec after the 5V supply has reached its minimum regulation level, and at TTL high level thereafter as long as outputs are within regulation.
   - At turn–off, the Power Good signal must drop to a TTL low level before any output drops below its regulation limits.
   - The driver must be capable of driving 400 microamps or sinking 5 milliamps. The rise time/fall time must be less than 1 usec., 10—90%
4. The +5V rise time (10%-90%) shall be 3 msec to 100 msec with a maximum slope of 0.75 volts/msec for voltages above 1.5 volts for all loadings.
5. All supply voltages shall track within 50 msec of each other measured at the 50% point.

D.1.2 Onboard 3.3V Regulator

There is a 3.3 volt regulator circuit on the example planar to support the CPU and the 660 Bridge. Note that the 3.3v on the PCI bus slots is sourced via the power supply connector, not the onboard 3.3v regulator.

Table D-3. Specifications for 3.3V Regulator on the Motherboard

Specification	Value
Output Voltage	3.3 V $\pm$ 3%
Output Current	0.01 A to 5 A
Input voltage	4.75 V to 5.25 V
Pass element maximum case temperature	110 °C
Tracking	In regulation <1ms after +5 reaches 4.75V.
Overcurrent	No current limit feature

D.2 Physical Design Rules

These guidelines are given to aid designers with the physical design phase of their 100 MHz PPC 603e MCM planar. The guidelines are not intended to replace good physical design practices for the signal types and frequencies discussed, but to supplement standard practice by pointing out sensitive and critical areas. Some discussion of the IBM implementation of the example planar is also included to establish the context for the wiring guidelines.

The example planar was developed by adapting the Harley Reference Design to meet the needs of the MCM. The physical design rules for the example planar are identical to those for Harley except for any changes which are contained in the following areas.

D.2.1 Construction

The general construction of the example planar is shown in Figure D-1. It is constructed with two high frequency signal layers in the center, two power planes, and two external general purpose signal layers.

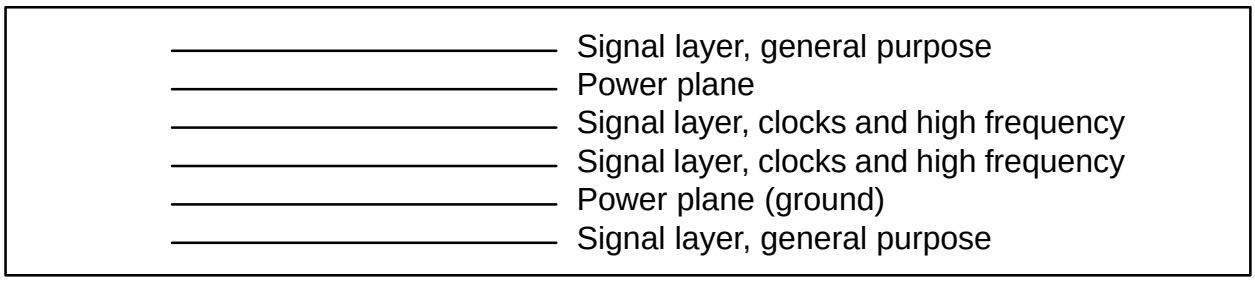


Figure D-1. Signal and Power Layers

A top view of a typical wiring channel, as implemented on the example planar, is shown in Figure D-2 (all dimensions are shown in inches). Minimum trace width is .006” (at 1:1) and minimum space width is .004” (at 1:1).

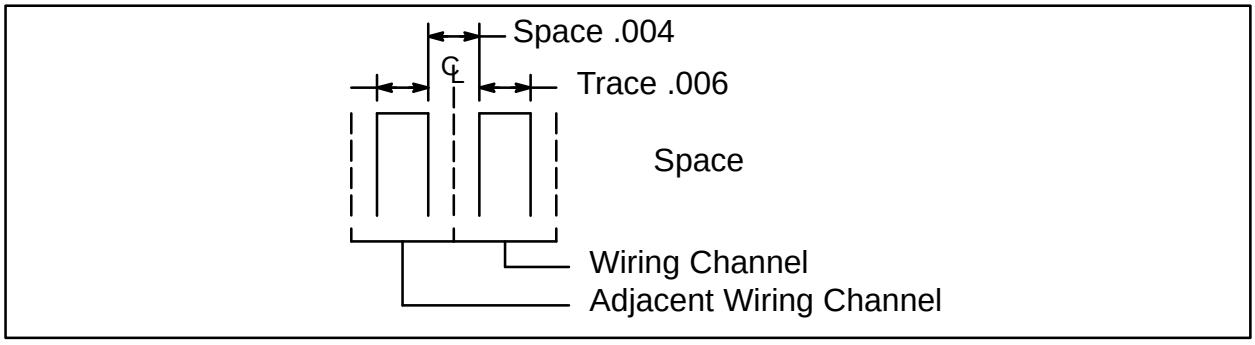
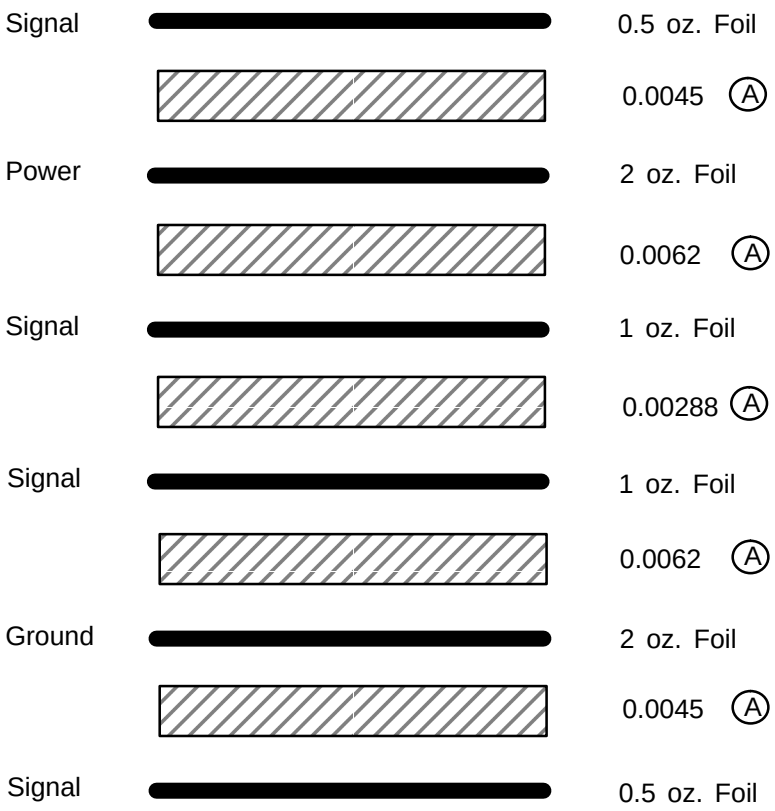
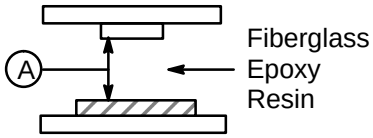


Figure D-2. Typical Wiring Channel Top View



Notes:



(B) All dimensions in inches

(C) Trace to ground impedance 70 Ω ± 10%

(D) Finished signal trace width: 0.00425

(E) Overall thickness: 0.060
after plating: 0.062

(F) Plating 7070

Figure D-3. PowerPC 603/604 Board Fabrication

D.2.2 General Wiring Guidelines

1 A power (ground or voltage) plane split occurs where there is a discontinuity in the plane. As shown in Figure D-4, route wires across splits in a power plane in the most perpendicular manner possible. Do not run wires parallel to the split in close proximity to the split.

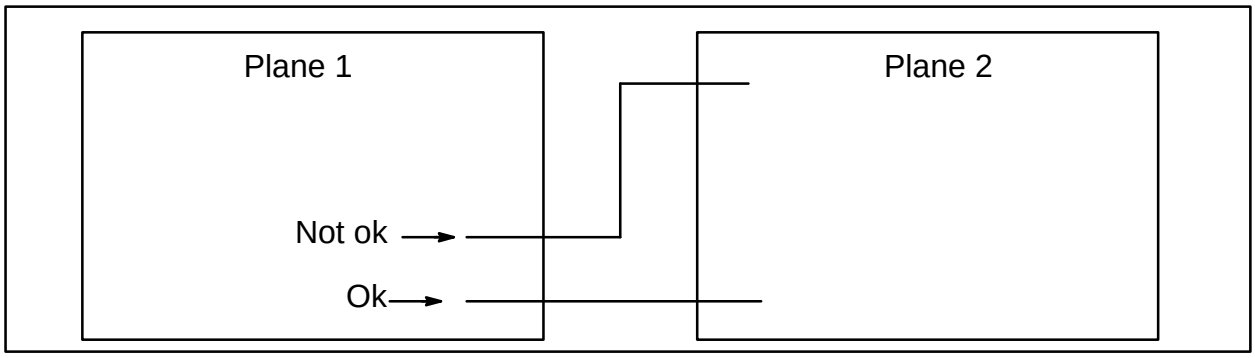


Figure D-4. Power Plane Split

2 Minimize the number of wires on the top surface of the board that cross under the clock generator. Do not run any wires close to the crystal connections.

3 If a wire is routed near a via which is part of a clock net, there must be at least one vacant wiring channel between the wire and the clock via.

4 Several groups of nets require special attention to ensure correct system operation. They are listed below in order of the importance of meeting the design rules that are suggested for that group. For example, ensuring that the clock nets are routed according to the design rules suggested in Section D.3 is more important than ensuring that the PCI bus nets are routed according to the design rules suggested in Section D.4. The ideal system design will meet all of the suggested design rules, but this information is included to guide the designer in case some tradeoffs have to be evaluated.

- Clock nets.
- CPU bus nets and timing critical nets.
- PCI bus nets.
- Noise sensitive nets.
- Other nets.

D.3 CPU Bus Nets

1 Make the CPU bus nets either 2–node nets or daisy-chained. Stubs and star fanouts are not allowed.

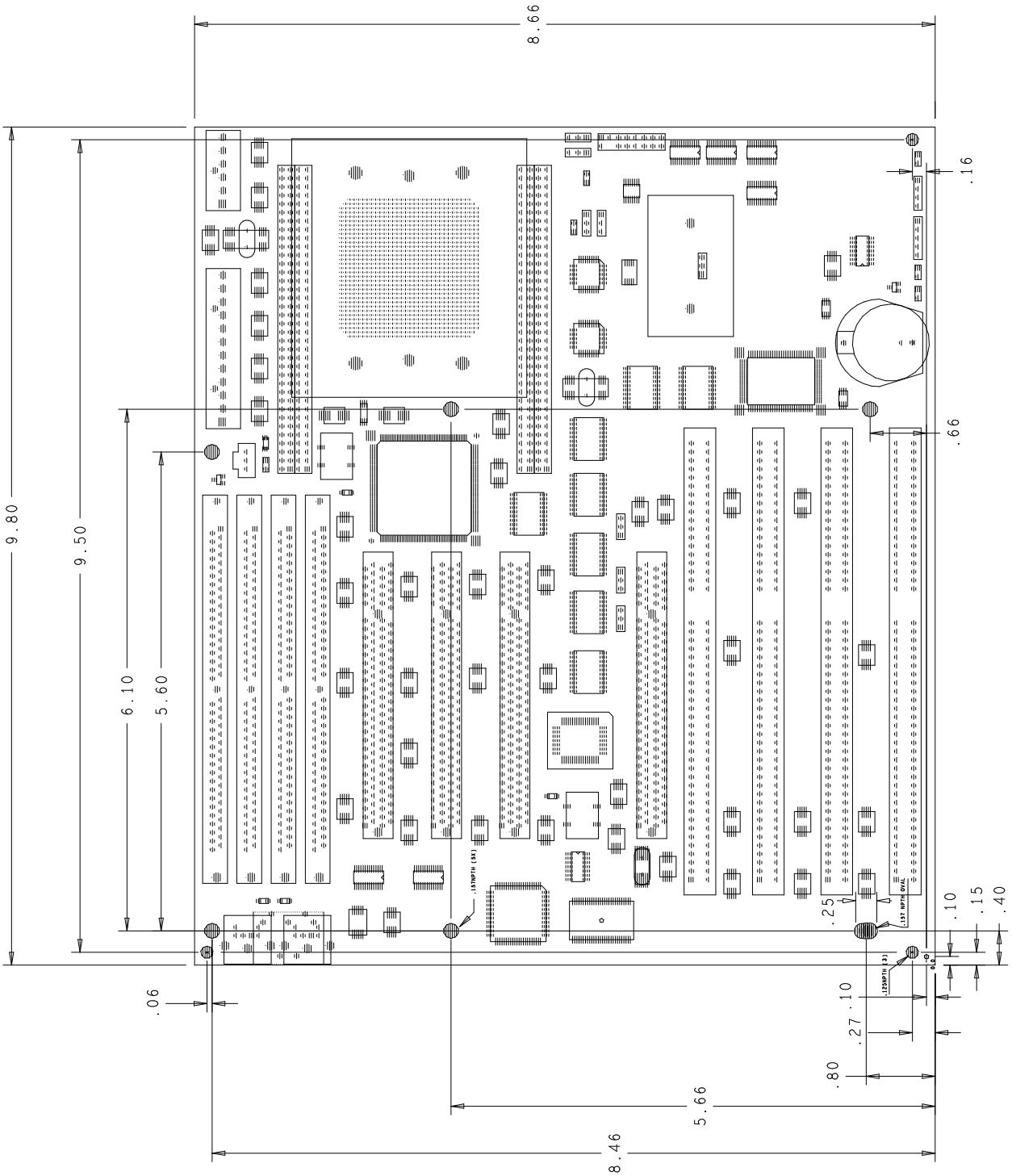
2 Route nets so as to minimize noise reception. Make these nets as short as possible.

D.4 PCI Bus Nets

1 Daisy chain the PCI bus nets. Stubs and star fanouts are not allowed.

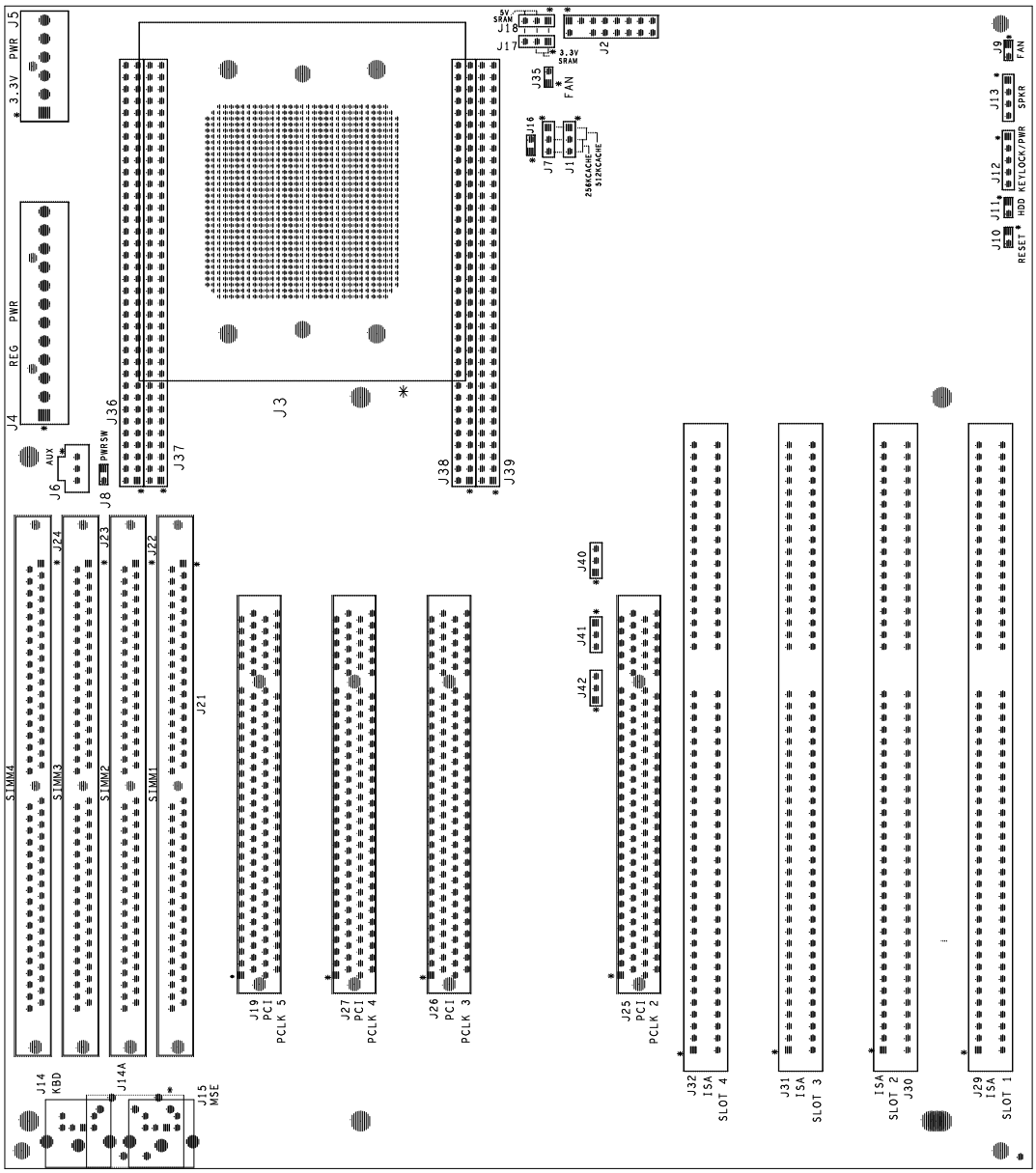
2 Route these nets so as to minimize noise reception and timing delays. Make these nets as short as possible.

D.5 Example Planar Mechanical

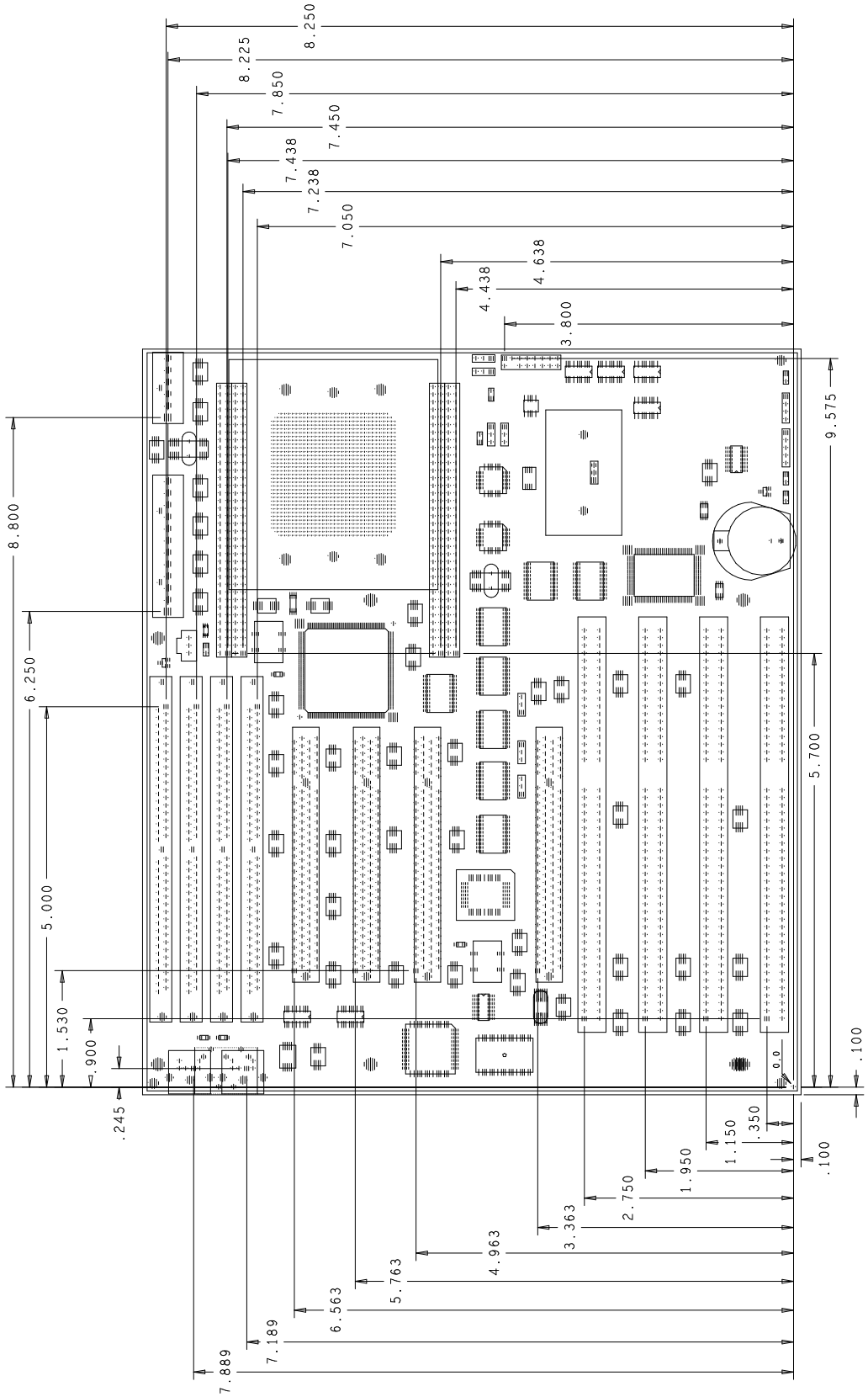


D.5.1 Example Planar Connectors

		X	Y
J1	CACHE SELECT	8575	3800
J2	RISCWATCH	9575	3800
J3	MCM SOCKET	8050	6050
J4	REG. POWER	6225	8225
J5	3.3V POWER	8800	8225
J6	AUX	5900	7950
J7	CACHE SELECT	8575	3975
J8	PWR SWITCH	5750	7225
J9	FAN	9325	100
J10	RESET	7750	100
J11	HDD	8000	100
J12	KEYLOCK/PWR	8600	100
J13	SPEAKER	8925	100
J14	KEYBOARD	245	7889
J14A	ALTERNATE	400	7164
J15	MOUSE	245	7189
J16	DELAY CONN.	8525	4125
J17	3.3V SRAM	9400	4075
J18	5V SRAM	9575	4075
J19	PCLK5	1530	6563
J21	SIMM 1	5000	7050
J22	SIMM 2	5000	7450
J23	SIMM 3	5000	7850
J24	SIMM 4	5000	8250
J25	PCLK2	1530	3363
J26	PCLK3	1530	4963
J27	PCLK4	1530	5763
J29	ISASLOT 1	900	350
J30	ISASLOT 2	900	1150
J31	ISASLOT 3	900	1950
J32	ISASLOT 4	900	2750
J35	FAN	9100	3975
J36	EMULATOR	5700	7438
J37	EMULATOR	5700	7238
J38	EMULATOR	5700	4638
J39	EMULATOR	5700	4438
J40	JUMPER	5025	3575
J41	JUMPER	4400	3575
J42	JUMPER	3950	3575



D.5.2 Example Planar Connector Locations



D.5.3 Keyboard Connector J14

The keyboard connector uses a 6-pin miniature DIN connector (see Figure D-5) Pins are assigned as shown in Table D-4 (as viewed from the back of the machine).

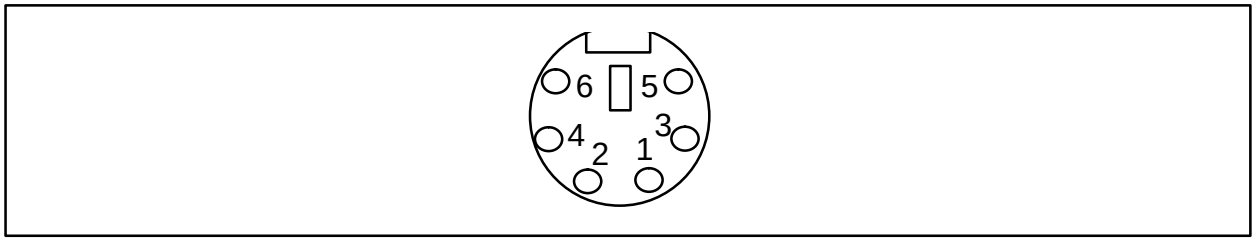


Figure D-5.The Keyboard Connector

Table D-4. Keyboard Connector Pin Assignments

Pin	I/O	Signal Name
1	I/O	DATA
2	NA	n/c
3	NA	GROUND
4	NA	+ 5V DC
5	I/O	CLOCK
6	NA	n/c
M1,2,3	NA	Shield Ground

D.5.4 Alternate Keyboard Connector J14A

The alternate keyboard connector uses a 5-pin miniature DIN connector (see Figure D-6) Pins are assigned as shown in Table D-5 (as viewed from the back of the machine).

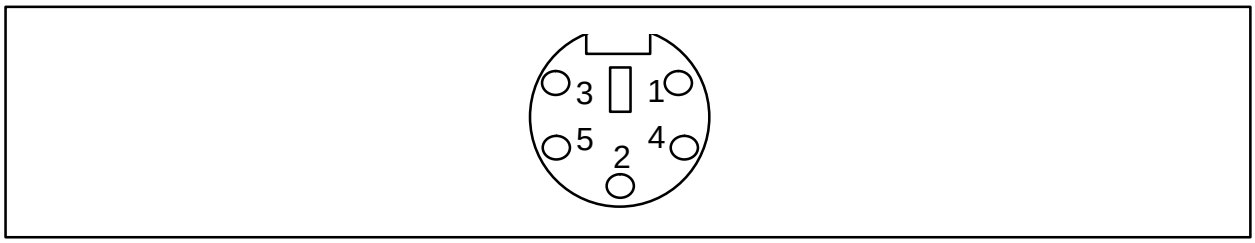


Figure D-6.The Alternate Keyboard Connector

Table D-5. Alternate Keyboard Connector Pin Assignments

Pin	Signal Name
1	CLOCK
2	DATA
3	n/c
4	GROUND
5	+ 5V DC
M1,2,3	Shield Ground

D.5.5 Mouse Connector J15

The mouse connector uses a 6-pin miniature DIN connector (see Figure D-7). Pins are assigned as shown in Table D-6 (as viewed from the back of the machine).

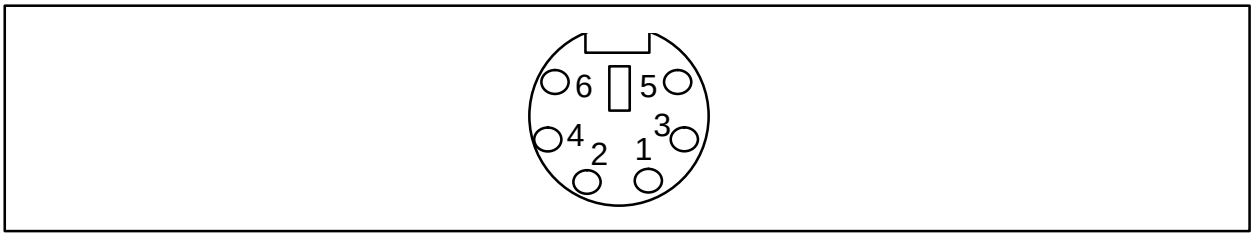


Figure D-7.The Mouse Connector

Table D-6. Mouse Connector Pin Assignments

Pin	I/O	Signal Name
1	I/O	DATA
2	NA	n/c
3	NA	GROUND
4	NA	+ 5V DC
5	I/O	CLOCK
6	NA	n/c
M1,2,3	NA	Shield Ground

D.5.6 Speaker Connector J13

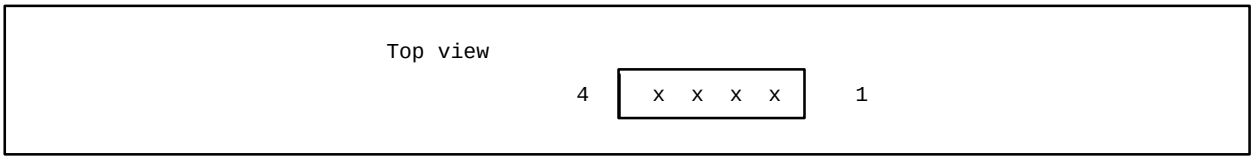


Figure D-8.1x4 Speaker Connector

Table D-7. Speaker Connector Pin Assignments

Pin No.	Signal Name
1	MINUS (–) INPUT TO SPEAKER
2	NO CONNECT
3	NO CONNECT
4	GND

D.5.7 Power Good LED/KEYLOCK# Connector J12

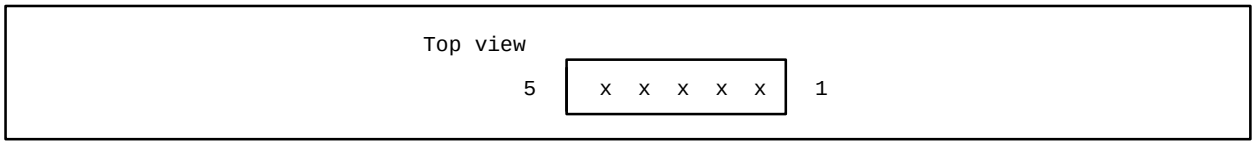


Figure D-9.1x5 Power Good LED Connector

Table D-8. Power Good LED Connector

Pin No.	Signal Name
1	LED_POWER_GOOD/RESET#
2	NO CONNECT
3	GND
4	KEYLOCK* (Not Used)
5	GND

D.5.8 HDD LED Connector J11 (1 x 2 Berg)

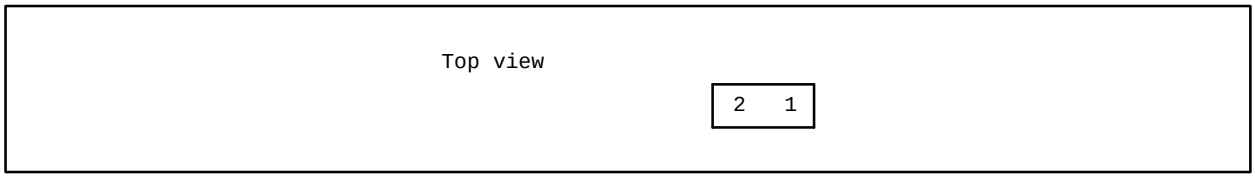


Figure D-10.1x2 HDD LED Connector

Table D-9. HDD LED Connector

Pin No.	Signal Name
1	+ LED VOLTAGE
2	HDD LED drive signal (low to drive LED)

D.5.9 Reset Switch Connector J10 (1 x 2 Berg)

Figure D-11.1x2 Reset Switch Connector

Table D-10. Reset Switch Connector

Pin No.	Signal Name
1	RESET N/O CONTACT (close to reset)
2	GROUND

D.5.10 Fan Connector J9, J35

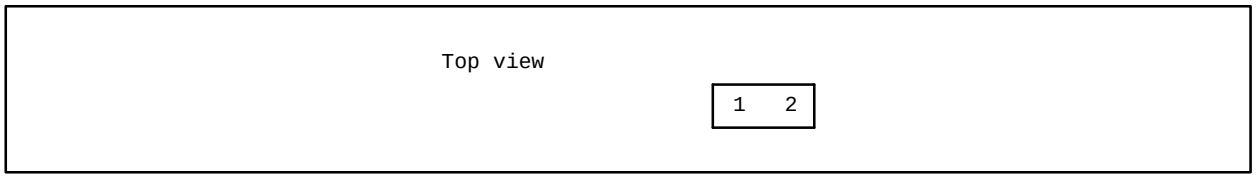


Figure D-12.1x2 Fan Connector

Table D-11. Fan Connector Pin Assignments

Pin No.	Signal Name
1	+12 VOLTS
2	GROUND

D.5.11 3.3V Power Connector J5

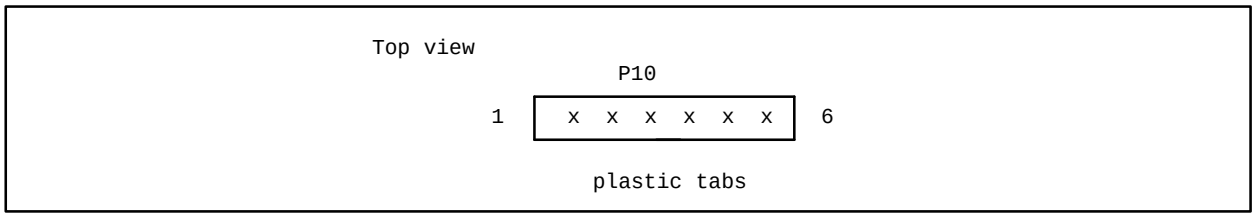


Figure D-13.1x6 3.3V Power Connector J5

Table D-12. 3.3V Power Connector J5 Pin Assignments

Pin No.	Signal Name
1	+3.3 V
2	+3.3 V
3	+3.3 V
4	GROUND
5	GROUND
6	GROUND

D.5.12 Power Connector J4

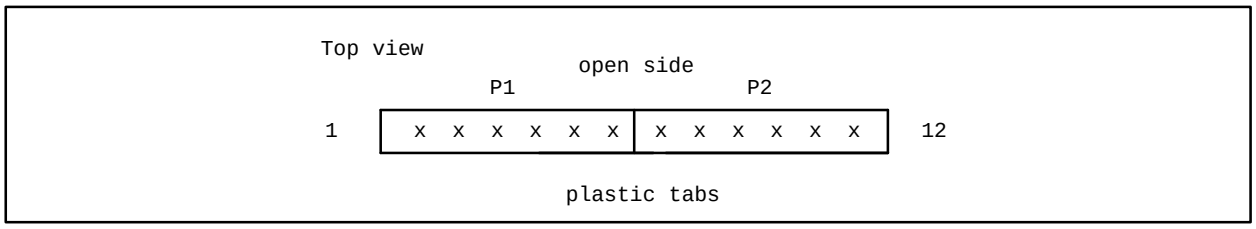


Figure D-14.1x12 Power Connector

Table D-13. Power Connector J4 Pin Assignments

Pin No.	Signal Name
1	POWER GOOD
2	+5 VOLTS
3	+12 VOLTS
4	–12 VOLTS
5, 6, 7, 8	GROUND
9, 10, 11, 12	–5 VOLTS

D.5.13 AUX5/ON-OFF Connector J6

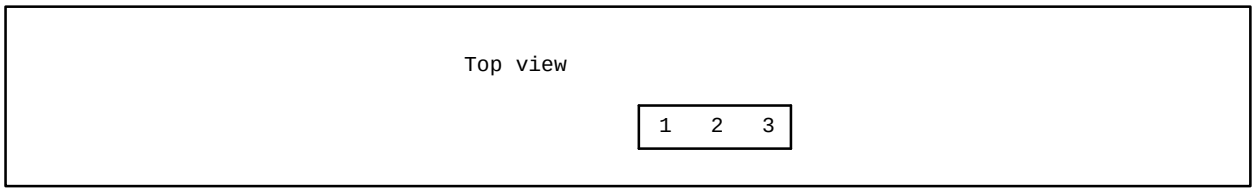


Figure D-15.AUX5/ON-OFF Connector

Table D-14. AUX5/ON-OFF Connector Pin Assignments

Pin No.	Signal Name
1	AUX +5V
2	ON/OFF
3	GROUND

D.5.14 PCI Connectors J19, J25, J26, and J27

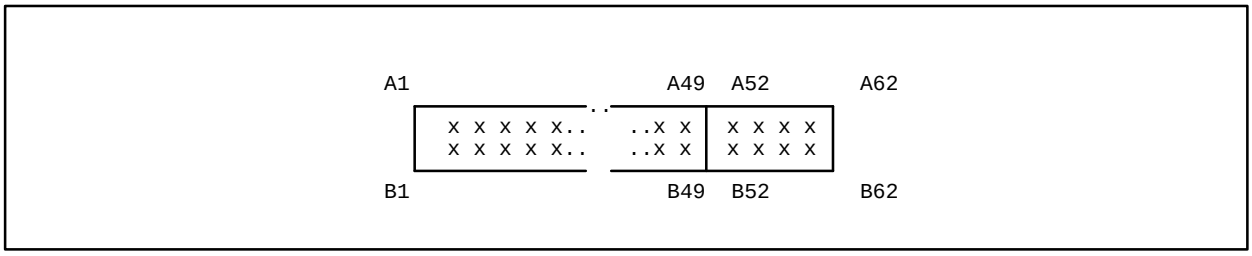


Figure D-16.PCI Connector

Table D-15. PCI Connector Pin Assignments

Pin	Function	Pin	Function
A1	TRST#	B1	–12 VOLTS#
A2	+12 VOLTS	B2	TCK
A3	TMS	B3	GROUND
A4	TDI	B4	TDO
A5	+5 VOLTS	B5	+5 VOLTS
A6	INTA#	B6	+5 VOLTS
A7	INTC#	B7	INTB#
A8	+5 VOLTS	B8	INTD#
A9	RESERVED	B9	PRESENT 1# *
A10	+5 VOLTS	B10	RESERVED
A11	RESERVED	B11	PRESENT 2# *
A12	GROUND	B12	GROUND
A13	GROUND	B13	GROUND
A14	RESERVED	B14	RESERVED
A15	RESET#	B15	GROUND
A16	+5 VOLTS	B16	CLK
A17	GNT#	B17	GROUND
A18	GROUND	B18	REQ#
A19	RESERVED	B19	+5 VOLTS
A20	A/D(30)	B20	A/D(31)

Table D-15. PCI Connector Pin Assignments (Continued)

Pin	Function	Pin	Function
A21	+3.3V	B21	A/D(29)
A22	A/D(28)	B22	GROUND
A23	A/D(26)	B23	A/D(27)
A24	GROUND	B24	A/D(25)
A25	A/D(24)	B25	+3.3V
A26	IDSEL	B26	C/BE#(3)
A27	+3.3V	B27	A/D(23)
A28	A/D(22)	B28	GROUND
A29	A/D(20)	B29	A/D(21)
A30	GROUND	B30	A/D(19)
A31	A/D(18)	B31	+3.3V
A32	A/D(16)	B32	A/D(17)
A33	+3.3V	B33	C/BE#(2)
A34	FRAME#	B34	GROUND
A35	GROUND	B35	IRDY#
A36	TRDY#	B36	+3.3V
A37	GROUND	B37	DEVSEL#
A38	STOP#	B38	GROUND
A39	+3.3V	B39	LOCK#
A40	SDONE	B40	PERR#
A41	SBO#	B41	+3.3V
A42	GROUND	B42	SERR#
A43	PAR	B43	+3.3V
A44	A/D(15)	B44	C/BE#(1)
A45	+3.3V	B45	A/D(14)
A46	A/D(13)	B46	GROUND
A47	A/D(11)	B47	A/D(12)
A48	GROUND	B48	A/D(10)
A49	A/D(9)	B49	GROUND
A50	<Key>	B50	<Key>
A51	<Key>	B51	<Key>
A52	C/BE#(0)	B52	A/D(8)
A53	+3.3V	B53	A/D(7)
A54	A/D(6)	B54	+3.3V
A55	A/D(4)	B55	A/D(5)
A56	GROUND	B56	A/D(3)
A57	A/D(2)	B57	GROUND
A58	A/D(0)	B58	A/D(1)
A59	+5 VOLTS	B59	+5 VOLTS
A60	REQ64#	B60	ACK64#
A61	+5 VOLTS	B61	+5 VOLTS
A62	+5 VOLTS	B62	+5 VOLTS

Notes:

***** The two card type bits, B9 and B11, are connected on the riser.

****** Int A-D, A6, A7, B7, and B8 are connected together on the riser.

D.5.15 ISA Connectors J29, J30, J31, J32

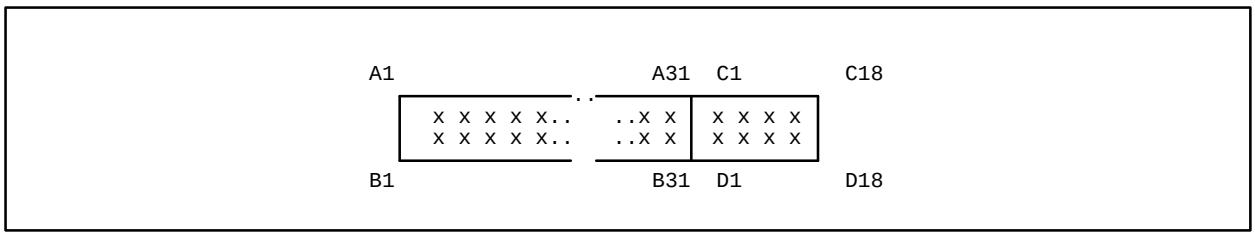


Figure D-17.ISA Connector

Table D-16. ISA Connector Pin Assignments

Pin	Function	Pin	Function
A1	IO CHCK#	B1	GROUND
A2	SD(7)	B2	RESET_DRV
A3	SD(6)	B3	+5 VOLTS
A4	SD(5)	B4	IRQ9
A5	SD(4)	B5	–5 VOLTS
A6	SD(3)	B6	DRQ2
A7	SD(2)	B7	–12 VOLTS
A8	SD(1)	B8	ZERO WS#
A9	SD(0)	B9	+12 VOLTS
A10	IO CHRDY	B10	GROUND
A11	AEN	B11	SMEMW#
A12	SA(19)	B12	SMEMR#
A13	SA(18)	B13	IOW#
A14	SA(17)	B14	IOR#
A15	SA(16)	B15	DACK3#
A16	SA(15)	B16	DRQ3
A17	SA(14)	B17	DACK1#
A18	SA(13)	B18	DRQ1
A19	SA(12)	B19	REFRESH
A20	SA(11)	B20	CLK
A21	SA(10)	B21	IRQ7
A22	SA(9)	B22	IRQ6
A23	SA(8)	B23	IRQ5
A24	SA(7)	B24	IRQ4
A25	SA(6)	B25	IRQ3
A26	SA(5)	B26	DACK2#
A27	SA(4)	B27	T/C
A28	SA(3)	B28	BALE
A29	SA(2)	B29	+5 VOLTS
A30	SA(1)	B30	Oscillator
A31	SA(0)	B31	GROUND
C1	SBHE#	D1	MEMCS16#
C2	LA(23)	D2	IO CS16#
C3	LA(22)	D3	IRQ10
C4	LA(21)	D4	IRQ11
C5	LA(20)	D5	IRQ12

Table D-16. ISA Connector Pin Assignments (Continued)

Pin	Function	Pin	Function
C6	LA(19)	D6	IRQ15
C7	LA(18)	D7	IRQ14
C8	LA(17)	D8	DACK0#
C9	MEMR#	D9	DRQ0
C10	MEMW#	D10	DACK5#
C11	SD(8)	D11	DRQ5
C12	SD(9)	D12	DACK6#
C13	SD(10)	D13	DRQ6
C14	SD(11)	D14	DACK7#
C15	SD(12)	D15	DRQ7
C16	SD(13)	D16	+5 VOLTS
C17	SD(14)	D17	MASTER#
C18	SD(15)	D18	GROUND

D.5.16 DRAM SIMM Connectors J21, J22, J23, and J24

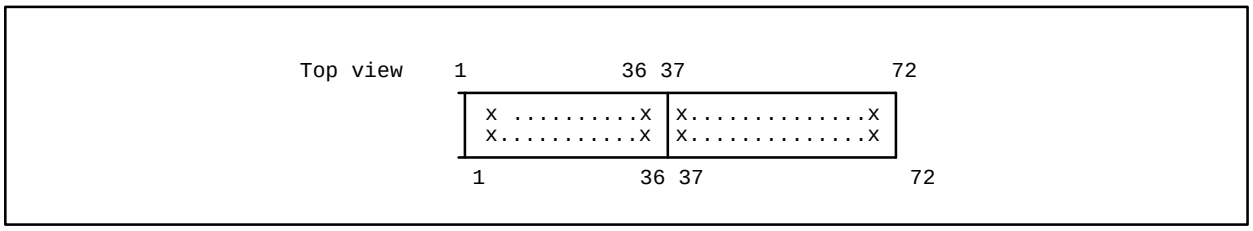


Figure D-18.DRAM SIMM Connector

Table D-17. DRAM SIMM Connector Pin Assignments

SIMM Pin	Motherboard Pin	Function
1	1	GROUND
2	2	DQ0
3	3	DQ18
4	4	DQ1
5	5	DQ19
6	6	DQ2
7	7	DQ20
8	8	DQ3
9	9	DQ21
10	10	+5 V
11	11	CASP
12	12	A0
13	13	A1
14	14	A2
15	15	A3
16	16	A4
17	17	A5
18	18	A6
19	19	A10

Table D-17. DRAM SIMM Connector Pin Assignments (Continued)

SIMM Pin	Motherboard Pin	Function
20	20	DQ4
21	21	DQ22
22	22	DQ5
23	23	DQ23
24	24	DQ6
25	25	DQ24
26	26	DQ7
27	27	DQ25
28	28	A7
29	29	BS0/A11
30	30	+5V
31	31	A8
32	32	A9
33	33	RAS3#
34	34	RAS2#
35	35	DQ26
36	36	DQ8
37	37	DQ17
38	38	DQ35
39	39	GROUND
40	40	CAS0#
41	41	CAS2#
42	42	CAS3#
43	43	CAS1#
44	44	RAS0#
45	45	RAS1#
46	46	BS1
47	47	WE#
48	48	RESD1
49	49	DQ9
50	50	DQ27
51	51	DQ10
52	52	DQ28
53	53	DQ11
54	54	DQ29
55	55	DQ12
56	56	DQ30
57	57	DQ13
58	58	DQ31
59	59	+5 V
60	60	DQ32
61	61	DQ14
62	62	DQ33
63	63	DQ15
64	64	DQ34

Table D-17. DRAM SIMM Connector Pin Assignments (Continued)

SIMM Pin	Motherboard Pin	Function
65	65	DQ16
66	66	BS2
67	67	PD1
68	68	PD2
69	69	PD3
70	70	PD4
71	71	BS3
72	72	GROUND

D.5.17 Power Switch Connector J8

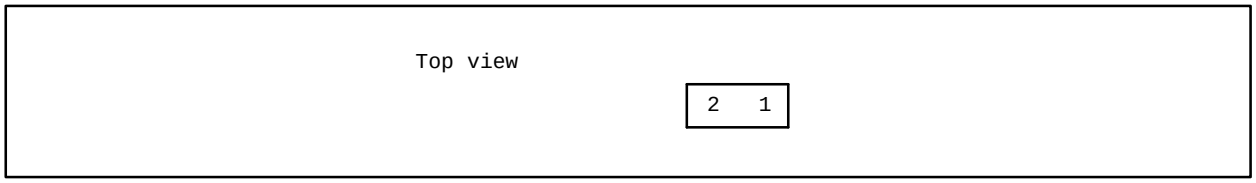


Figure D-19.1x2 Power Switch Connector

Table D-18. Power Switch Connector Pin Assignments

Pin No.	Signal Name
1	SWITCH_P1
2	SWITCH_GD

D.5.18 Power Up Configuration Connector J7

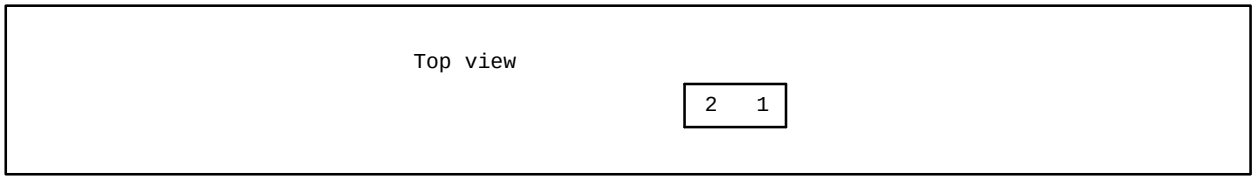


Figure D-20.1x2 Power Up Configuration Connector

Table D-19. Power Up Configuration Connector Pin Assignments

Pin No.	Signal Name
1	PWR_CFG1
2	PWR_CFG2

D.5.19 RISCWatch Connector J2

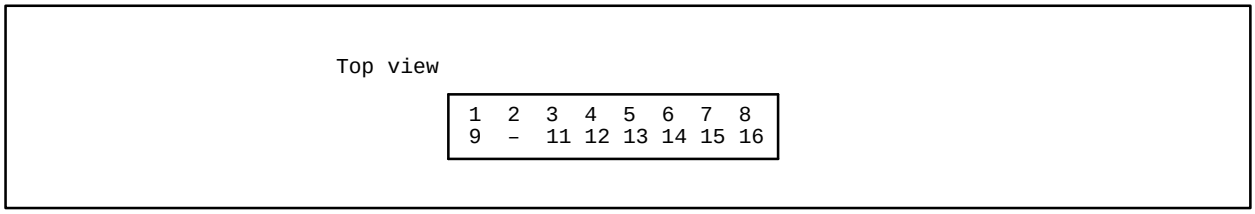


Figure D-21.2x8 RISCWatch Connector

Table D-20. RISCWatch Connector Pin Assignments

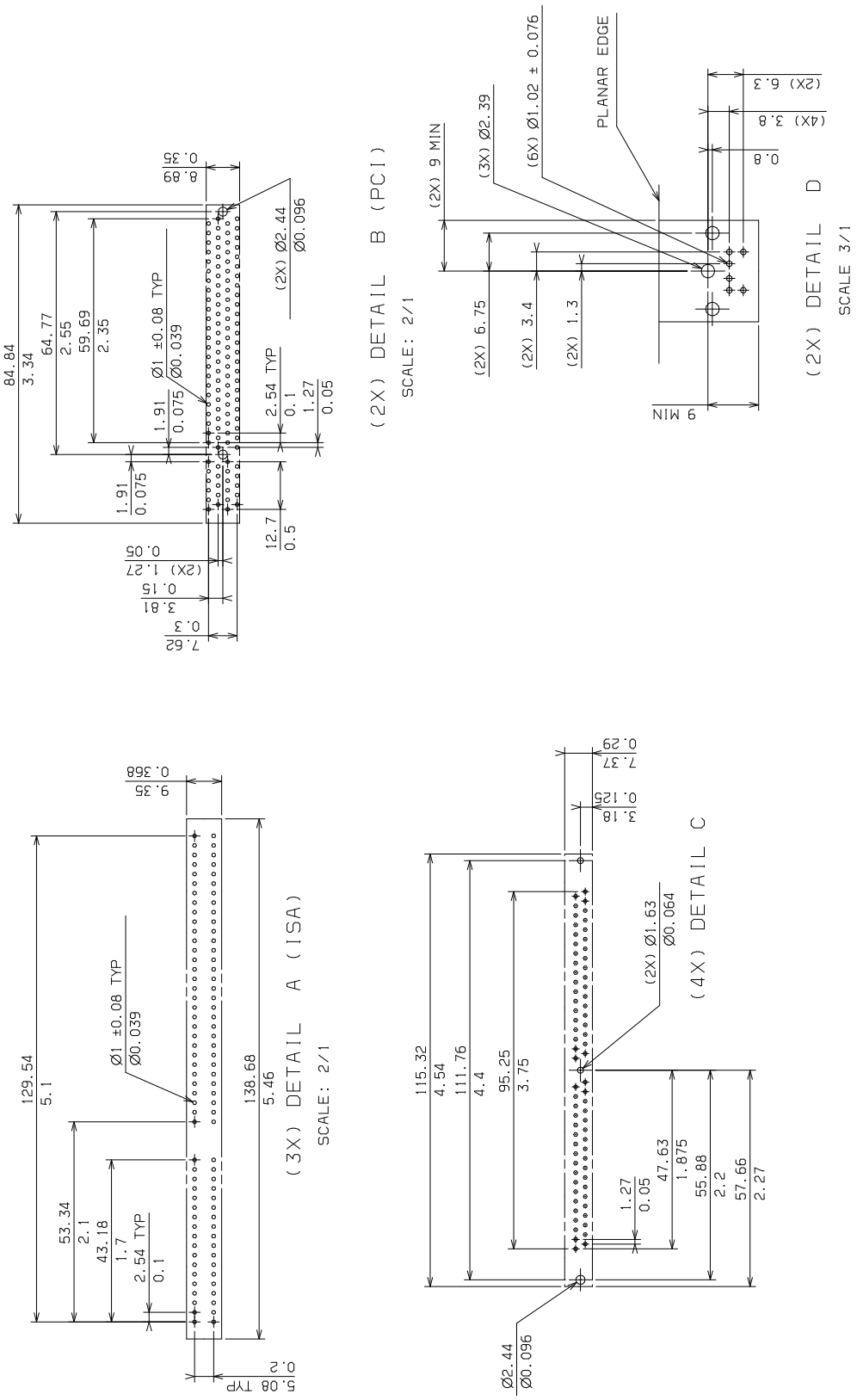
Pin No.	Signal Name
1	CHECK_STOP#
2	HDWR_RESET#
3	RESET_INTERRUPT#
4	CNTL/SCAN_DATA
5	SHIFT_CLK
6	+RUN/–BREAKPOINT
7	SCAN_IN
8	SCAN_OUT
9	GROUND
10	<Key>
11	GROUND
12	RESERVED
13	RESERVED
14	+5 VOLTS
15	OCS_OVERRIDE
16	RESERVED

D.5.20 Battery Connector BT2

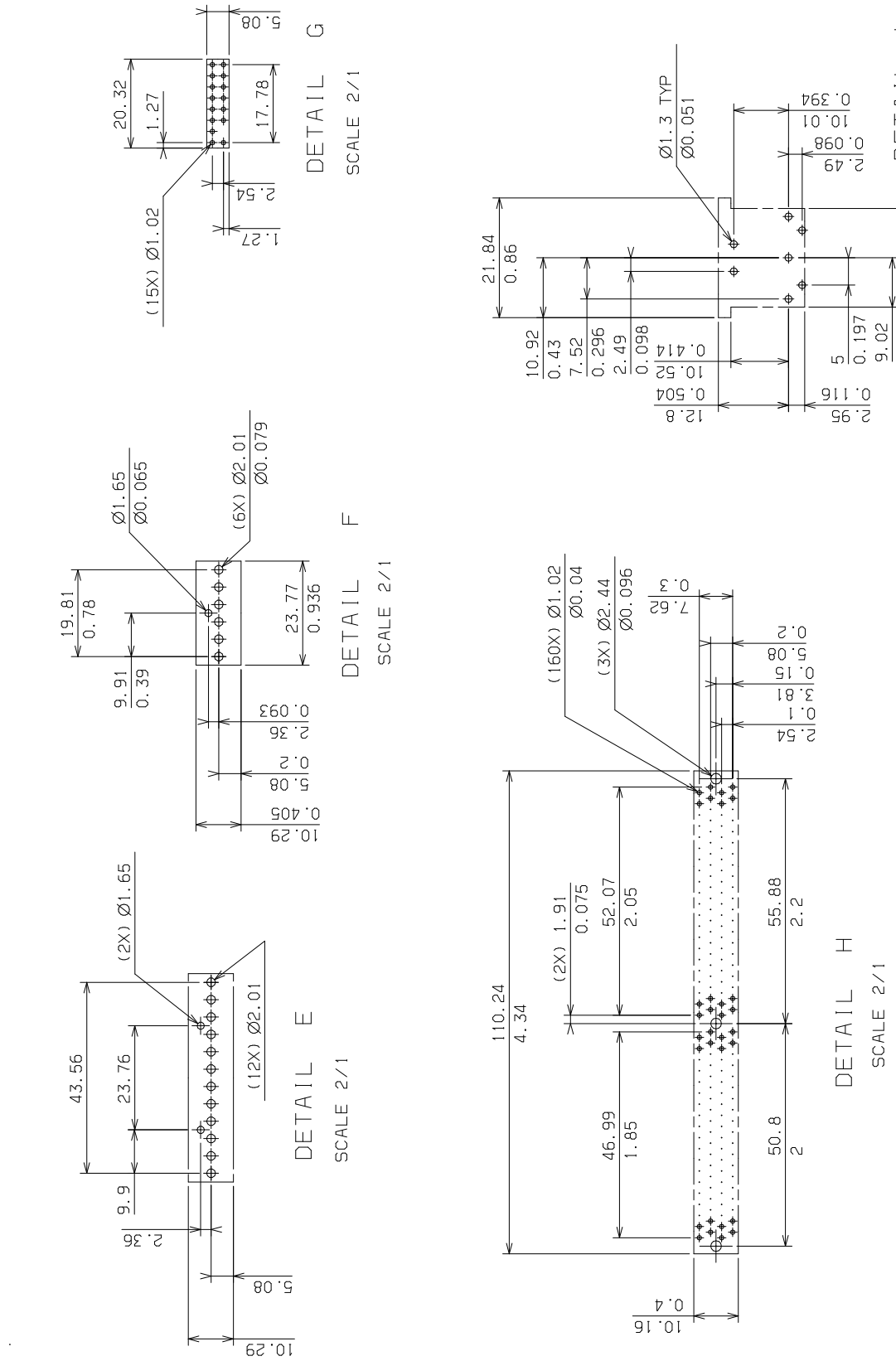
The battery type is CR2032 3 Volt.

Insert the battery with + side up.

D.5.21 MCM Board Connector Footprint #1



D.5.22 MCM Board Connector Footprint #2



D.6 Enclosure

The example planar is mechanically very similar to the Harley board. Enclosures for Harley should work for the example planar, but this has not been verified. The information in this section should be considered as tentative. The experienced designer will verify the appropriateness of an enclosure before specifying it.

The following venders supply enclosures:

Olson Metal Products Company Inc.
Attn: Michelle Seay
1903 N. Austin Street
Seguin, Texas 78155
1-800-951-9517 or (210) 379-7000

AT Desktop model number: CC300249
Medium Tower model number: CC400000

Altex Electronics
11342 IH-35 North
San Antonio, Texas
1-800-531-5367 or FAX (210) 637-3264

Mini Tower model number STC–05
Medium Tower model number STC–08
Full Tower model number STC–16

Mega-Tech Marketing Inc.
3900-D Drossett Dr.
Austin, Texas

Mini Tower model number A6601
Full Tower model number A5561

Note: IBM makes no recommendations regarding vendors of any components.

In planning the layout of an enclosure, the height of the items in Table D-21 should be considered.

Table D-21. Height Considerations

Item	Approximate Height
3.3V regulator heat sink	26.0 mm
SIMMs (seated)	28.4 mm
L2 SRAM SIMM (seated)	28.4 mm
MCM and mounting	

Appendix E
Bill of Materials

E.1 Planar Bill of Materials

Table E-1. Planar Bill of Materials

No	Part Name	Part Number	Reference Designator	Qty	Manufacturer Name	Manufacturer Part Number	JEDEC TYPE	Part Description
1	10MQ040_SOIC–BASE	87F4917	CR1,CR7	2	SANKEN	SFBP–54YL	D64	40V 1A SCHTK REC
2	29F040ROM_MECH_MECH–BASE	82G6496	X3	1	AMD	AM29F040–120JC	PART	512KX8 FLASH ROM
3	2N7002_SMD–BASE	31F2311	Q1	1	MOTOROLA	2N7002	SOT23	3 PIN FET TRANSISTOR
4	7406_SMD–BASE	17F7776	U3,U28	2	TI	7406	SO14	HEX INVERTER OC
5	74F08_SMD–BASE	61X9236	U1,U29	2	NATL	FO8	SO14	QUAD 2 INPUT & GATE
6	74F11_SMD–BASE	17F7745	U13	1	NATL	F11	SO14	TRI 3 INPUT AND GATE
7	74F125_SMD–BASE	68X2888	U16	1	NATL	74F125SCX	SO14	74F125 BUFFERS 3 STATE
8	74F244_SMD–BASE	6480438	U10,U11,U17–U20, U40	7	PHILIPS	74F244	SO20W	OCTAL BUFF/DRIVER
9	74F245_SMD–BASE	55X8091	U12	1	PHILIPS	74F245	SO20W	OCTAL TRANSCEIVER
10	74F74_SMD–BASE	61X9238	U21	1	NATL	F74	SO14	DUAL”D”FF W/CLEAR & PRESET
11	74HCT14_SMD–BASE	37F9034	U2	1	PHILIPS	74HCT14	SO14	74HCT14 SCHMT TRIGGER INV
12	8042H_SMD–BASE	1054195	U27	1	INTEL	8042H	PLCC44	KEYBOARD CONTROLLER
13	8G4756_SMD–BASE	08G4756	CR6	1	MOTOROLA	MMBD914 LT1	SOT23	70V 200MA SWC DIODE
14	BATTERY_MECH–BASE	15F8409	B1	1	SONY	CR2032	PART	BATTERY 3.3V
15	BERG1X2_DIP–BASE	6181127	J8–J11,J16,J35	6	BERG	69190–502	BERG1X2	1X2 100MIL HEADER VERTICAL
16	BERG1X4_DIP–BASE	6359315	J13	1	BERG	69190–504	BERG1X4	1X4 100MIL HEADER VERTICAL
17	BERG1X5_DIP–BASE	88G4908	J12	1	AMP	104345–3	BERG1X5	BERGSTICK 1X5
18	CAPACITOR–0.001UF,20%	98F1292	C129–C148	20	KYOCERA	08055C102 KAT2A	SMC0805	CAPACITOR

Table E-1. Planar Bill of Materials (Continued)

No	Part Name	Part Number	Reference Designator	Qty	Manufacturer Name	Manufacturer Part Number	JEDEC TYPE	Part Description
19	CAPACITOR–0.01UF,20%	41F0313	C3–C5,C28–C31, C33–C37,C39,C40, C46–C50,C52,C53, C57,C58,C61,C80–C82,C84,C86,C93, C95,C117–C120, C124,C127,C151, C157–C164,C167–C169,C172–C174, C203–C206,C208–C210,C212–C215, C217–C220,C222–C225,C255–C257, C259,C269–C274	81	KYOCERA	0805X103 M2B05	SMC0805	CAPACITOR
20	CAPACITOR–0.1UF,20%	41F0316	C9,C43,C91,C92, C94	5	KYOCERA	0805Y104 Z1B05	SMC0805	CAPACITOR
21	CAPACITOR–10UF,20%	71F7911	C8	1	NEC	TESVEC 1C106M12R	71F7911	CAPACITOR
22	CAPACITOR–2200PF,20%	42G3220	C32,C83,C85,C123, C125	5	MURATA	GRM40X7R 222J050AD	SMC0805	CAPACITOR
23	CAPACITOR–33UF/20%/16V	57G9281	C202,C207,C211, C216,C221	5	KEMET	T491D336 M016AS	CAP33UF3SMT	CAPACITOR
24	CAPACITOR–68PF,20%	62G4724	C87–C90,	4	KYOCERA	08055A680 KAT2	SMC0805	CAPACITOR
25	CAPACITOR–DO_NOT_POP, 20%	–NONE–	C1,C2,C6,C7,C10–C21,C70,C71,C98, C99,C149,C150, C152–C154,C156, C226	27	NONE	NONE	SMC0805	CAPACITOR
26	CHANDRA_SMD–BASE	SKT_100	M1	1	ALTERA	100 QFP SOCKET	100QFP	GTP W/128 MACROCELLS
27	CONNBATT_KELPIE_CONN–BASE	33F8027	M5	1	KELPIE	K17–BH–001	CONN_33F8027	BATTERY HOLDER
28	CONNBERG2X36_DIP– BASE	N_MOLEX	J36–J39	4	MOLEX	15–44–4536	BERG2X36	2X36 MOLEX PCB CONN
29	CONNDIN5–DO_NOT_POP	–NONE–	J14A	1	NONE	NONE	CONN_5DIN	AT KEYBOARD CONNECTOR
30	CONNMDIN6–CONNMDIN6	15F6890	J14,J15	2	AMP	749180–1	CONN_15F6890	6 POS CIRCULAR MINI DIN
31	CONNPOWER2_DIP–BASE	N_BURND	J5	1	BURNDY	GTC6R–1	CONN_1X6	1X6 0 156 CL FRET LCK HDR
32	CONNPOWER_DIP–BASE	55X8085	J4	1	MOLEX	15–48–0212	CONN_55X8085	1X12 0 156 CL FRET LCK HDR
33	CONN_BATTERY–SONY_NO_POP	19G2441	M3	1	SONY		CONN_19G2441	BATTERY HOLDER
34	CONN_BERG1X3_DIP–BASE	1501831	J1,J7,J17,J18,J40–J42	7	BERG	69190–503	BERG1X3	1X3 100MIL HEADER VERTICAL
35	CONN_ISA_DIP–BASE	6137473	J29–J32	4	AMP	645169–4	ISA2X49	2X49 ISA CONNECTOR
36	CONN_PCI_DIP–BASE	72G0316	J19,J25–J27	4	AMP	646255–1	PCI2X605V	2X60 32 BIT PCI CONNECTOR
37	CONN_SIMM72_DIP–BASE	64F5806	J21–J24	4	AMP	822032–4	SIMM72	72 PIN SIMM CONNECTOR
38	CRYSTAL_2PIN–32.768KHZ	03G9527	Y3	1	EPSON	MC405–32.768KHZ–6PF	XTALSMT1	CRYSTAL
39	CRYSTL–DO_NOT_POP	–NONE–	Y2,Y4	2	NONE	NONE	XTALSMT2	CRYSTAL
40	DO–NOT–POP_PLCC20_PLCC20–BASE	–NONE–	S3	1	NONE	NONE	PLCC20	DO–NOT–POP
41	DS1385_SMD–BASE	70G6764	U5	1	DALLAS	DS1385S	SO28W	RTC+ 4KX8SRAM
42	ELCAP–100UF, 10%/16V	75G8253	C110	1	SPRAGUE	293D107X 96R3D2T	SMC2816	CAPACITOR

Table E-1. Planar Bill of Materials (Continued)

No	Part Name	Part Number	Reference Designator	Qty	Manufacturer Name	Manufacturer Part Number	JEDEC TYPE	Part Description
43	ELCAP–33UF, 20%/16V	57G9281	C27,C38,C112–C116,C121,C122,C165,C166,C170,C171,C175–C183,C187–C198,C261–C263	37	KEMET	T491D336MO16AS	CAP33UF3SMT	CAPACITOR
44	EPM5130FP_SMD–BASE	05H0966	X2	1	ALTERA	EPM5130–QC–100–1	PART	GTP W/128 MACROCELLS
45	ESP_CONN_CONN–BASE	42F6867	J2	1	BERG	79282–516	CONN_42F6867	2X8 PIN HEADER CONN
46	F_BEAD_BEAD–BASE	26F4865	FB1,FB4–FB6	4	TDK	HF50ACB–321611T	SMC1206	FERRITE BEAD
47	IRFZ44_SMD–BASE	03G9500	Q6	1	IR	IRFZ44	TO220X	TRANSISTOR 50V 35A
48	LT1431REG_DIP–BASE	31F2428	U4	1	LINEARTECH	LT1431CS8	SO8	VOLT REGULATOR
49	MTGHOLE–DO_NOT_POP	–NONE–	MH1,MH3–MH5,MH7,MH8	6			157TOOL	
50	OSCLR–14.3181MHZ	87F5263	Y1	1	EPSON	SG–615P–14.31818MC	OSCSMT4	OSCLR
51	OSCLR–24.0MHZ	87F5265	Y5	1	EPSON	SG–615P–24.0000MC	OSCSMT4	OSCLR
52	PAL_20–SKT_19G5840	19G5840	S1	1	AMP	3-822269-1	PLCC20	SOCKET
53	PAL_MECH_MECH–BASE	05H0958	X5	1	AMD	PALCE16V8H–5JC–5	PART	PALCE16V8H–5JC–5
54	PART–JUMPER1X2	92F1420	X1,X4	2	AMP	530153-2	PART	JUMPER 1X2
55	PIN1089_DIP–BASE	60G8498	J3	1	IBM	CUSTOM	MCM33X33SKT	1089 PIN CGB SOCKET
56	PLCC32SKT_SMD–BASE	10G7624	M2	1	AMP	821977–1	PLCC32SKT	32 PIN PLCC SOCKET
57	POLYSWITCH_SMD–BASE	34G3113	F1	1	RAYCHEM	SMD100	POLYSWITCH	TAPE RESISTOR
58	POWER1X3_DIP–BASE	65G3724	J6	1	MOLEX	705–43–0037	POWER1X3	AUX POWER CONNECTOR
59	REGHSINK_DIP–BASE	8185352	M4	1	AAVID	533722B22552	REGHSINK	HEATSINK VOLTREG
60	RESISTOR–0,5%	98F1665	R14,R15,R17–R19,R69,R70,R72,R95,R129,R130,R135,R470,R471,R473	15	PANASONIC	ERJ8GVJ0R	SMC0805	RESISTOR
61	RESISTOR–1.5K,5%	98F1741	R436	1	ROHM	MCR10EZHLJW152	SMC0805	RESISTOR
62	RESISTOR–10,5%	58F1831	R40,R82,R85,R87,R89,R96,R97	7	PANASONIC	ERJ6GVYJ100S	SMC0805	RESISTOR
63	RESISTOR–100,5%	41F0328	R38,R39,R101,R107,R108,R153,R154,R176,R190,R192,R194,R238,R240,R365,R366,R485	16	PANASONIC	ERJ6VJ101S	SMC0805	RESISTOR
64	RESISTOR–10K,5%	41F0337	R1,R5–R8,R10,R13,R43,R74–R76,R78,R80,R81,R90–R93,R99,R102,R111–R113,R119,R138–R145,R147,R148,R155–R166,R174,R237,R253–R260,R287–R351,R364,R443,R488–R495,R497,R510	133	PANASONIC	ERJ6GVJ103S	SMC0805	RESISTOR
65	RESISTOR–12.7K,1%	40G7066	R512	1	PANASONIC	ERJ–6VNF1272S	SMC0805	RESISTOR

Table E-1. Planar Bill of Materials (Continued)

No	Part Name	Part Number	Reference Designator	Qty	Manufacturer Name	Manufacturer Part Number	JEDEC TYPE	Part Description
66	RESISTOR–150,5%	98F1671	R123	1	ROHM	MCR10EZH MJW151	SMC0805	RESISTOR
67	RESISTOR–1K,5%	41F0333	R12,R21,R28,R29, R31–R36,R41,R44, R47,R55,R77,R100, R230,R239,R280, R505,R513	21	PANASONIC	ERJ6GVJ 102S	SMC0805	RESISTOR
68	RESISTOR–2.7K,5%	09G9748	R261–R272	12	PANASONIC	ERJ–6GVYJ 272S	SMC0805	RESISTOR
69	RESISTOR–200,1%	40G6920	R4	1	PANASONIC	ERJ–6VNF 2000S	SMC0805	RESISTOR
70	RESISTOR–200,5%	98F1424	R73	1	PANASONIC	ERJ–6GEYJ 201V	SMC0805	RESISTOR
71	RESISTOR–22,5%	98F1736	R56,R88,R177, R178	4	PANASONIC	ERJ6GVYJ 220S	SMC0805	RESISTOR
72	RESISTOR–220K,5%	61F2952	R122	1	PANASONIC	ERJ6GVJ 224S	SMC0805	RESISTOR
73	RESISTOR–249,1%	40G7233	R437	1	PANASONIC	ERJ6VNF 2490S	SMC0805	RESISTOR
74	RESISTOR–3.9K,5%	42G3067	R120	1	PANASONIC	ERJ6GVYJ 392S	SMC0805	RESISTOR
75	RESISTOR–300,5%	98F1674	R103,R106,R225, R236,R241,R251, R281–R286	12	ROHM	MCR10EZH MJW301	SMC0805	RESISTOR
76	RESISTOR–33,5%	41F0327	R22–R27,R30,R65, R67,R68,R71,R83, R84,R86,R104, R105,R226–R229, R243,R250	22	PANASONIC	ERJ6GVYJ 330S	SMC0805	RESISTOR
77	RESISTOR–4.7K,5%	41F0336	R231–R235,R273–R279	12	PANASONIC	ERJ–6GVJ 472S	SMC0805	RESISTOR
78	RESISTOR–4.99K,1%	40G7034	R511	1	PANASONIC	ERJ6VNF 4991S	SMC0805	RESISTOR
79	RESISTOR–470K,5%	03G9709	R124	1	ROHM	MCR10EZH LJW474	SMC0805	RESISTOR
80	RESISTOR–5.6K,5%	98F1737	R352–R358	7	PANASONIC	ERJ6GVJ 562S	SMC0805	RESISTOR
81	RESISTOR–510,5%	41F0331	R118,R245	2	PANASONIC	ERJ6GVYJ 511S	SMC0805	RESISTOR
82	RESISTOR–620,5%	61F2960	R20	1	PANASONIC	ERJ6GVJ 621S	SMC0805	RESISTOR
83	RESISTOR–75,5%	61F2961	R79,R359–R362	5	PANASONIC	ERJ6GVJ 750S	SMC0805	RESISTOR
84	RESISTOR–80.6,1%	40G6887	R9	1	PANASONIC	ERJ–6VNF 80R6S	SMC0805	RESISTOR
85	RESISTOR–DO_NOT_POP,5%	–NONE–	R2,R3,R11,R16, R37,R42,R45,R46, R54,R57,R58,R62, R66,R94,R98,R121, R146,R149–R152, R189,R191,R193, R440,R441,R451, R472	28	NONE	NONE	SMC0805	RESISTOR
86	RLS4148_SOIC–BASE	87F4920	CR2	1	ROHM	RLS4148	MELF	40V 1A SCHTK REC
87	S82378ZB_SMD–BASE	82G6542	U7	1	INTEL	S82378ZB	QFP208_5MM	PCI TO ISA BRIDGE CONT
88	XTAL–16.50MHZ	89G3833	Y2A,Y4A	2	ECLIPTEK	ECX–2900–16.500MHZ	CLP_XTAL	16.5 MHZ CRYSTAL
90	XTAL–DO_NOT_POP	–NONE–	Y3A	1	NONE	NONE	CLP_XTAL	NONE
Total				591				

Appendix F
Planar Schematics

This section contains the schematics of the Odyssey MCM planar. For schematics of the MCM, see Section 13.

The schematic pages are numbered separately from the rest of the MCM technical specification.

Page 50 of the planar schematics shows a PAL that is used only for development and factory testing of parts of the MCM. This device is not required in user systems, and can be completely removed from the circuit. Note that in normal operation, the PAL is not populated, and the nets that are connected to the PAL outputs are driven by other devices.

F.1 Component Placement

IBM MICROELECTRONICS

RELEASE 0.1

ODYSSEY PLANAR

FOR MCM

LAST_MODIFIED=Tue Apr 2 17:28:21 1996

EC LEVEL: XXXXXXXX

RELEASE DATE: XXXXXXXX

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IBM	COVER SHEET		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY			SHEET 1 OF 51

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***** CONTENTS *******

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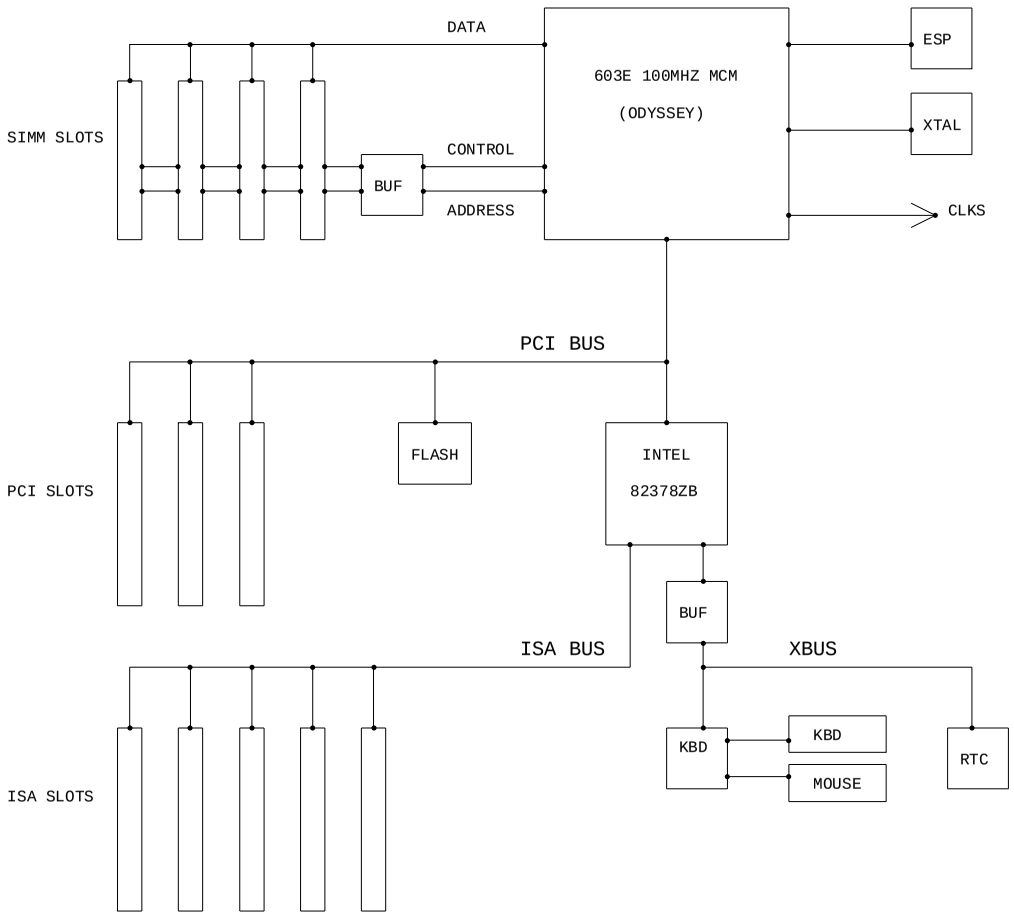
IBM	CONTENTS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Thu Feb 8 14:59:44 1996	SHEET 2 OF 51		



IBM

BLOCK DIAGRAM

SIZE	REVISION	DRWNG PART NUMBER
B	A	ODYSSEY

DRAWING ODYSSEY

LAST_MODIFIED=Tue Jan 30 17:23:53 1996

SHEET 3 OF 51

CRITICAL NETS INSTRUCTIONS

CRITICAL NET NAME	NET LENGTH	SHIELDING	OTHER CONSIDERATIONS
-sysclk/pclk_en	10.0	yes	(1) (5)-10005
-l2_bclk<4>	10.0	yes	(1) (4)-MAT1
l2_bclk<3..0>	6.0	yes	(1) (4)-MAT2
663_bclk	10.0	yes	(1) (5)-20000
664_bclk	10.0	yes	(1) (4)-MAT1
664_pci_clk	5.0	yes	(1) (5)-6000
pci_clk0	8.6	yes	(1) (5)-8700
pci_clk<4..1>	7.3	yes	(1) (4)-MAT3
isa_clk	asap	yes	(1)
buff_ps_power_good	asap	no	-
-man_reset_r	asap	no	-
-buff_man_reset	asap	no	-
-power_good/reset	asap	no	-
-sys_reset	asap	no	-
-pci_reset	asap	no	-
-hreset_60x	asap	no	-
-sreset_60x	asap	no	-
-esp_trst	asap	no	-
-hdwr_reset	asap	no	-
-esp_trst_60x	asap	no	-
resetdrv	asap	no	-
isa_reset	asap	no	-
a<31..0>	asap	no	(2)
d<63..0>	asap	no	(2)
dp<7..0>	asap	no	(2)
-aack_60x	asap	no	(2)
-artry_60x	asap	no	(2)
-br_60x	asap	no	(2)
-bg_60x	asap	no	(2)
-shd_6014	asap	no	(2)
-ts_60x	asap	no	(2)
-xats_60x	asap	no	(2)
tt<4..0>	asap	no	(2)
tsiz<2..0>	asap	no	(2)
-tbst_60x	asap	no	(2)
-gbl_60x	asap	no	(2)
-drtry_60x	asap	no	(2)
-ta_60x	asap	no	(2)
-tea_60x	asap	no	(2)
-ckstp_out_60x	asap	no	-
-int_60x	asap	no	-
-dpe_60x	asap	no	-
-mcp_6034	asap	no	-
-smi_6034	asap	no	-
esp_tms_60x	asap	no	-
esp_tck_60x	asap	no	-
esp_tdi_60x	asap	no	-
esp_tdo_60x	asap	no	-
halted/run_nstop	asap	no	-
sram_ads/addr0	asap	no	-
sram_cnt_en/addr1	asap	no	-
sram_ale	asap	no	-
-sram_we	asap	no	-
-sram_oe	asap	no	-
tag_match	asap	no	-
-tag_we	asap	no	-
tag_valid	asap	no	-
-tar_clear	asap	no	-
ad<31..0>	asap	no	(3)
-pci_frame	asap	no	(3)
-pci_trdy	asap	no	(3)
-pci_irdy	asap	no	(3)
-pci_stop	asap	no	(3)
-pci_devsel	asap	no	(3)
-pci_perr	asap	no	(3)
-pci_serr	asap	no	(3)
-pci_c/be<3..0>	asap	no	(3)
-pci_lock	asap	no	(3)
pci_par	asap	no	(3)

NOTE :-
(1) All nets should be in the inner layer & daisy chained whereever required.
(2) All the nets should be daisy chained.
The wiring order is :
U4 - U33 - U32 - U5 - U37 - U38 - J3.
(3) All the nets should be daisy chained.
The wiring order is :
M2 - M3 - U4 - U5 - U7 - J25 - J26 - J27 - J28.
(4) Matched Length group name.
(5) Max Net length.

CHANGE HISTORY

V0.1A 07/28/95 .... DRAFT

IBM

CRITICAL NETS
CHANGE HISTORY

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B	A	ODYSSEY

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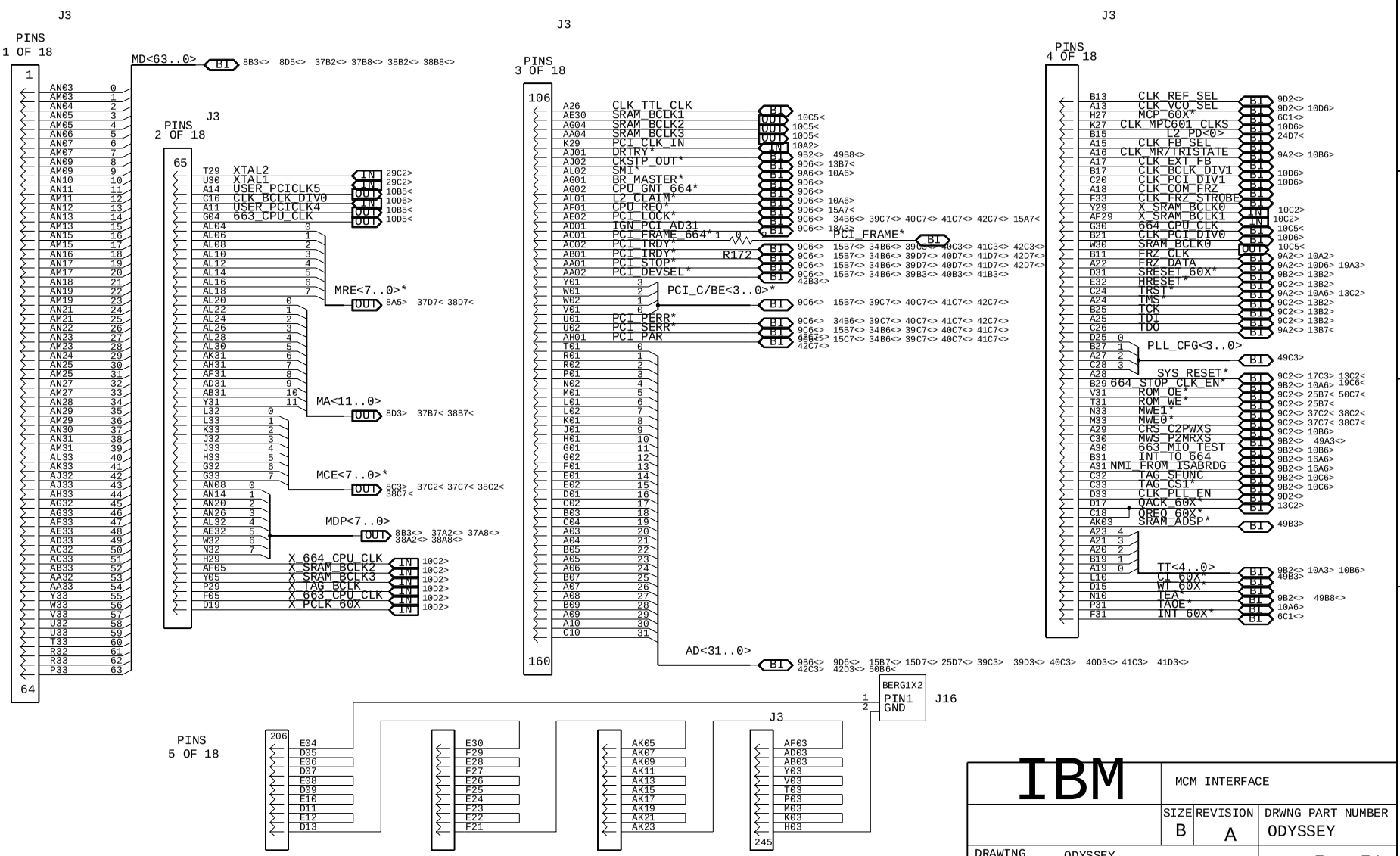
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1 OF 18
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J3
PINS
2 OF 18
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MA<11..0>
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MDP<7..0>
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X_SRAM_BCLK3
X_TAG_BCLK
X_663_CPU_CLK
X_PCLK_60X
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R172
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SYS_RESET*
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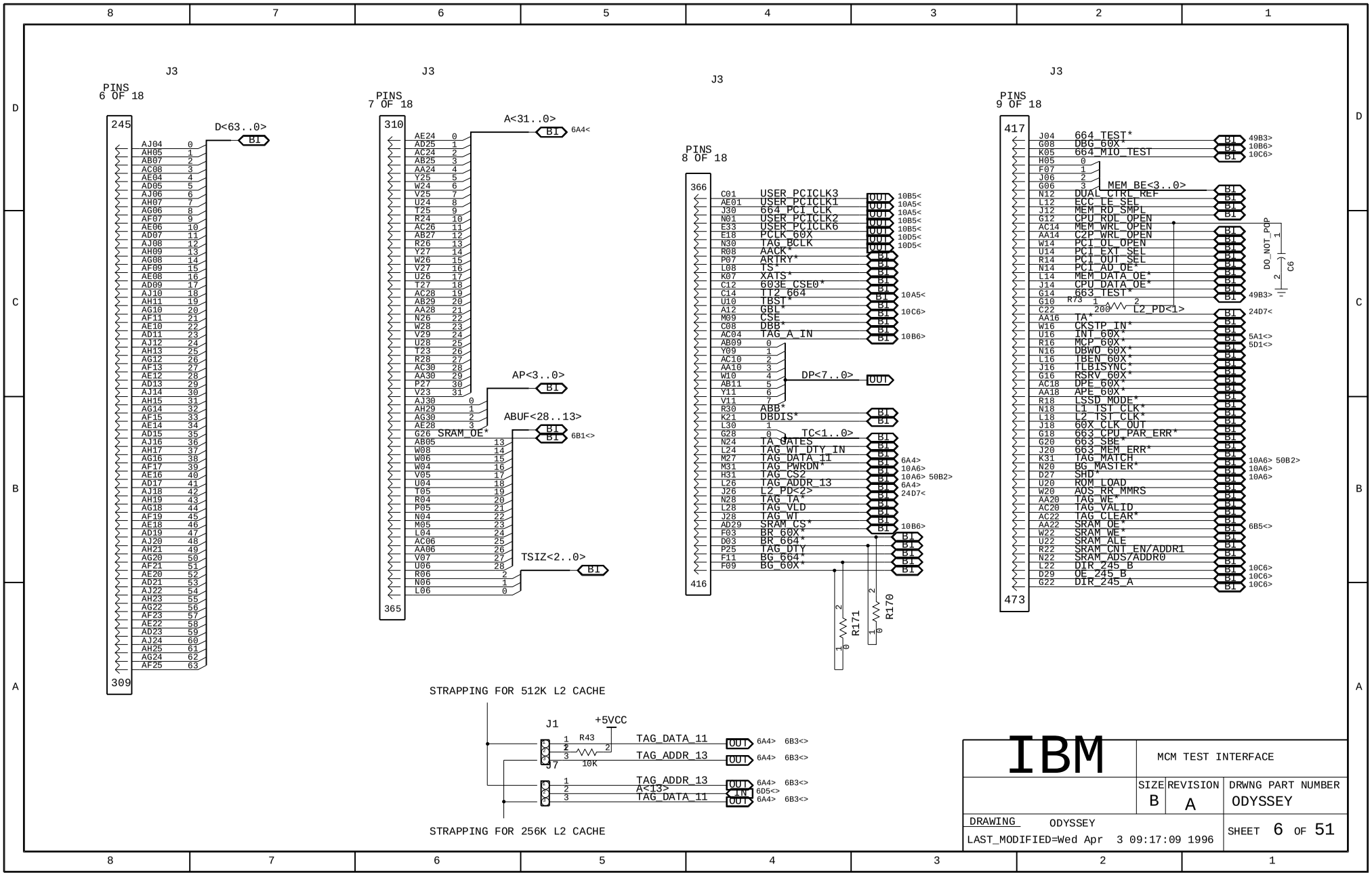
BERG1X2
PIN1
GND
J3
PINS
5 OF 18
IBM
MCM INTERFACE
SIZE
B
REVISION
A
DRWNG PART NUMBER
ODYSSEY
DRAWING
ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:17:04 1996
SHEET 5 OF 51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309
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B1
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AH05 1
AB07 2
AC08 3
AE04 4
AD05 5
AJ06 6
AH07 7
AG06 8
AF07 9
AE06 10
AD07 11
AJ08 12
AH09 13
AG08 14
AF09 15
AE08 16
AD09 17
AJ10 18
AH11 19
AG10 20
AF11 21
AE10 22
AD11 23
AJ12 24
AH13 25
AG12 26
AF13 27
AE12 28
AD13 29
AJ14 30
AH15 31
AG14 32
AF15 33
AE14 34
AD15 35
AJ16 36
AH17 37
AG16 38
AF17 39
AE16 40
AD17 41
AJ18 42
AH19 43
AG18 44
AF19 45
AE18 46
AD19 47
AJ20 48
AH21 49
AG20 50
AF21 51
AE20 52
AD21 53
AJ22 54
AH23 55
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AD23 59
AJ24 60
AH25 61
AG24 62
AF25 63
J3
PINS
7 OF 18
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365
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AE24 0
AD25 1
AC24 2
AB25 3
AA24 4
Y25 5
W24 6
V25 7
U24 8
T25 9
R24 10
AC26 11
AB27 12
AB29 20
AA28 21
N26 22
W28 23
V29 24
U28 25
T23 26
R28 27
AC30 28
AA30 29
P27 30
V23 31
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AJ30 0
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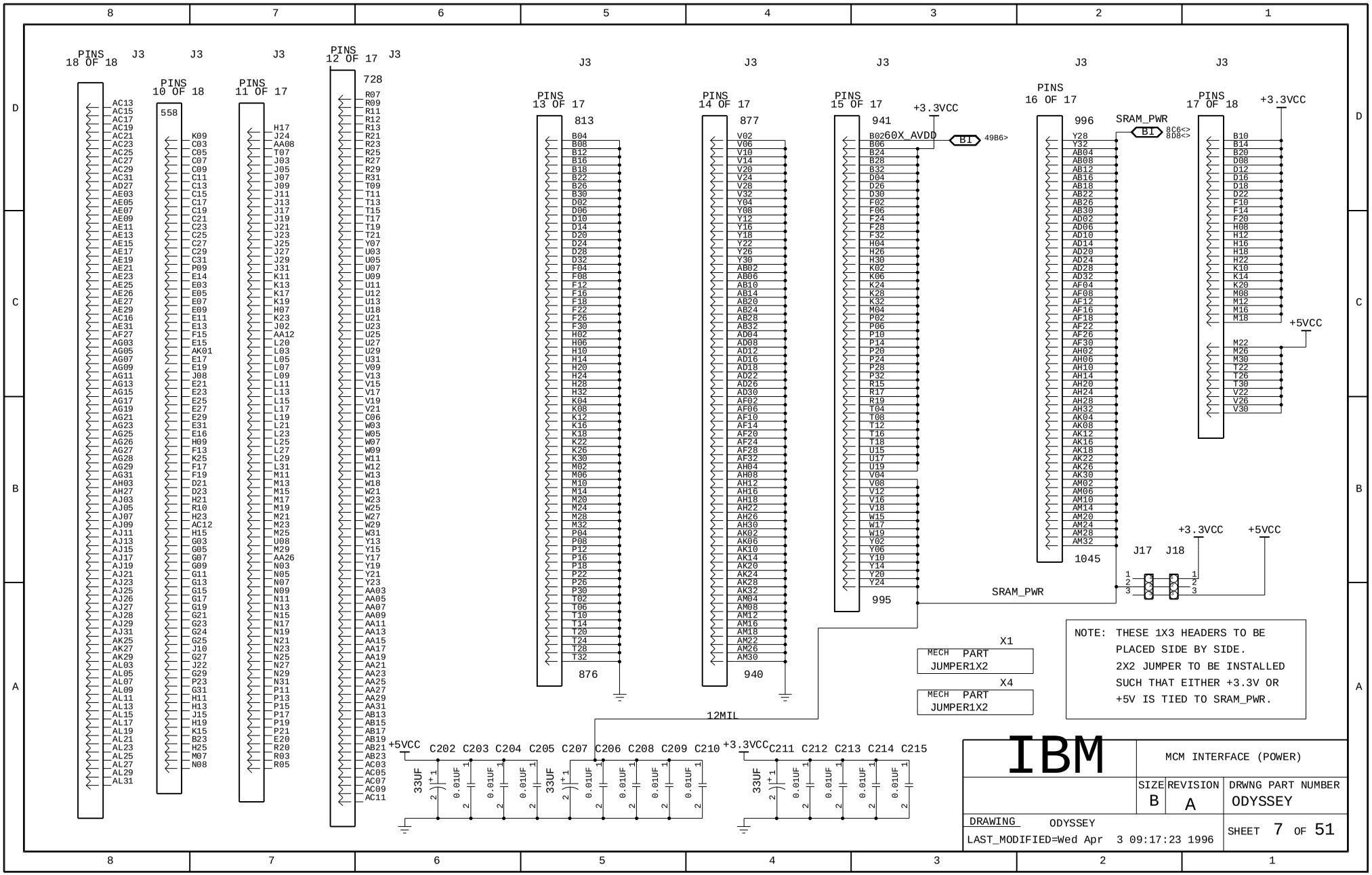
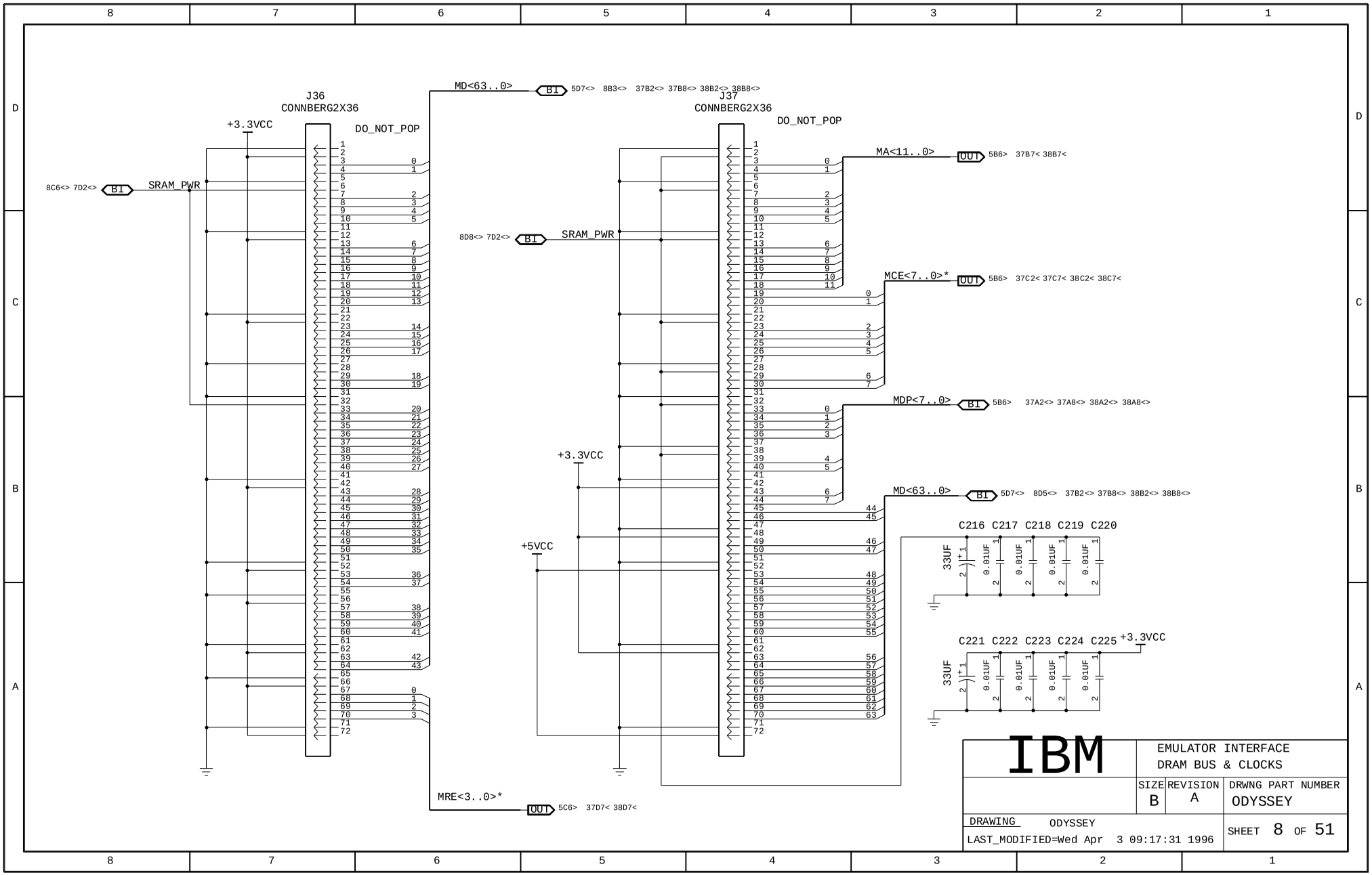
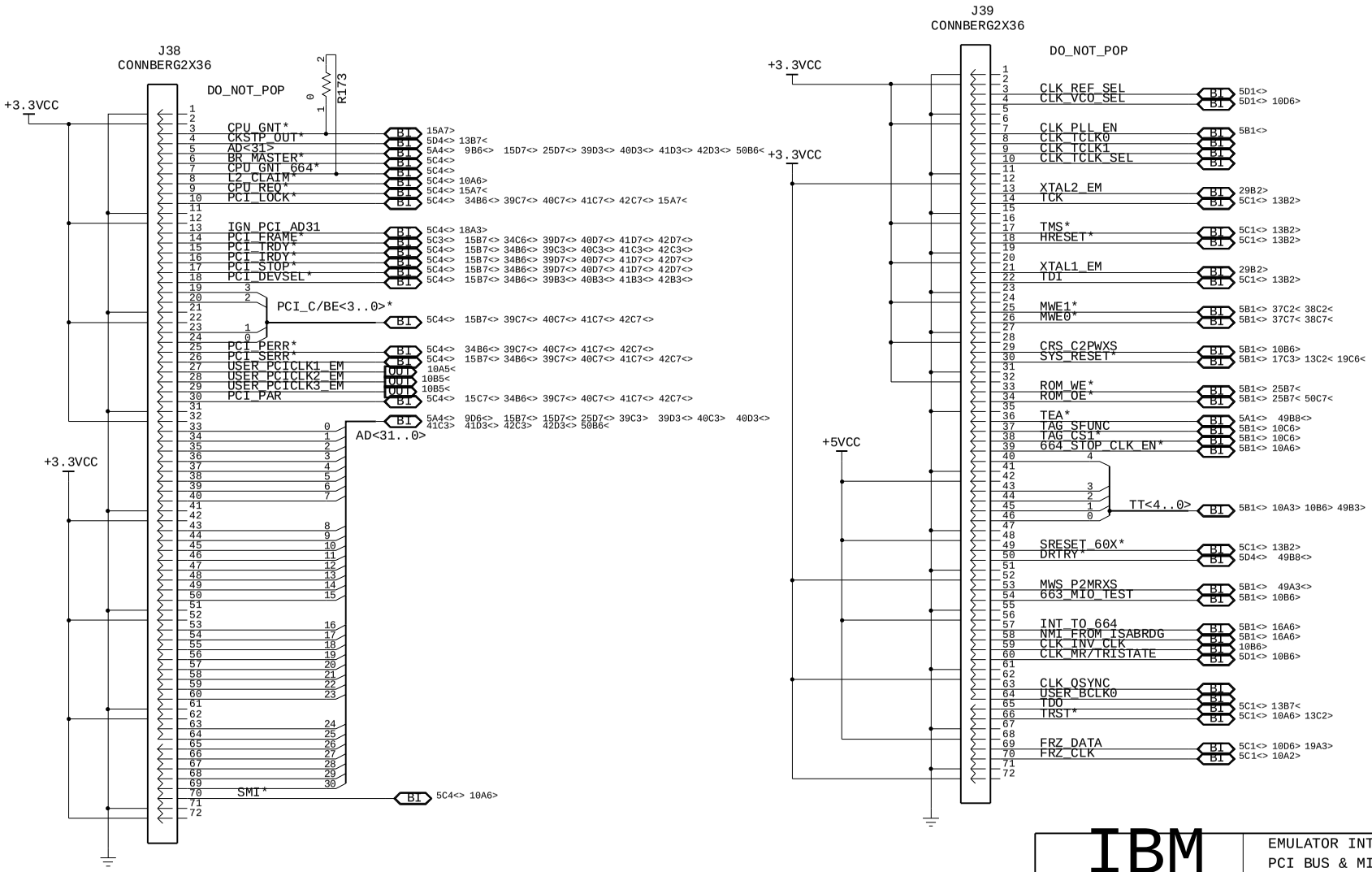
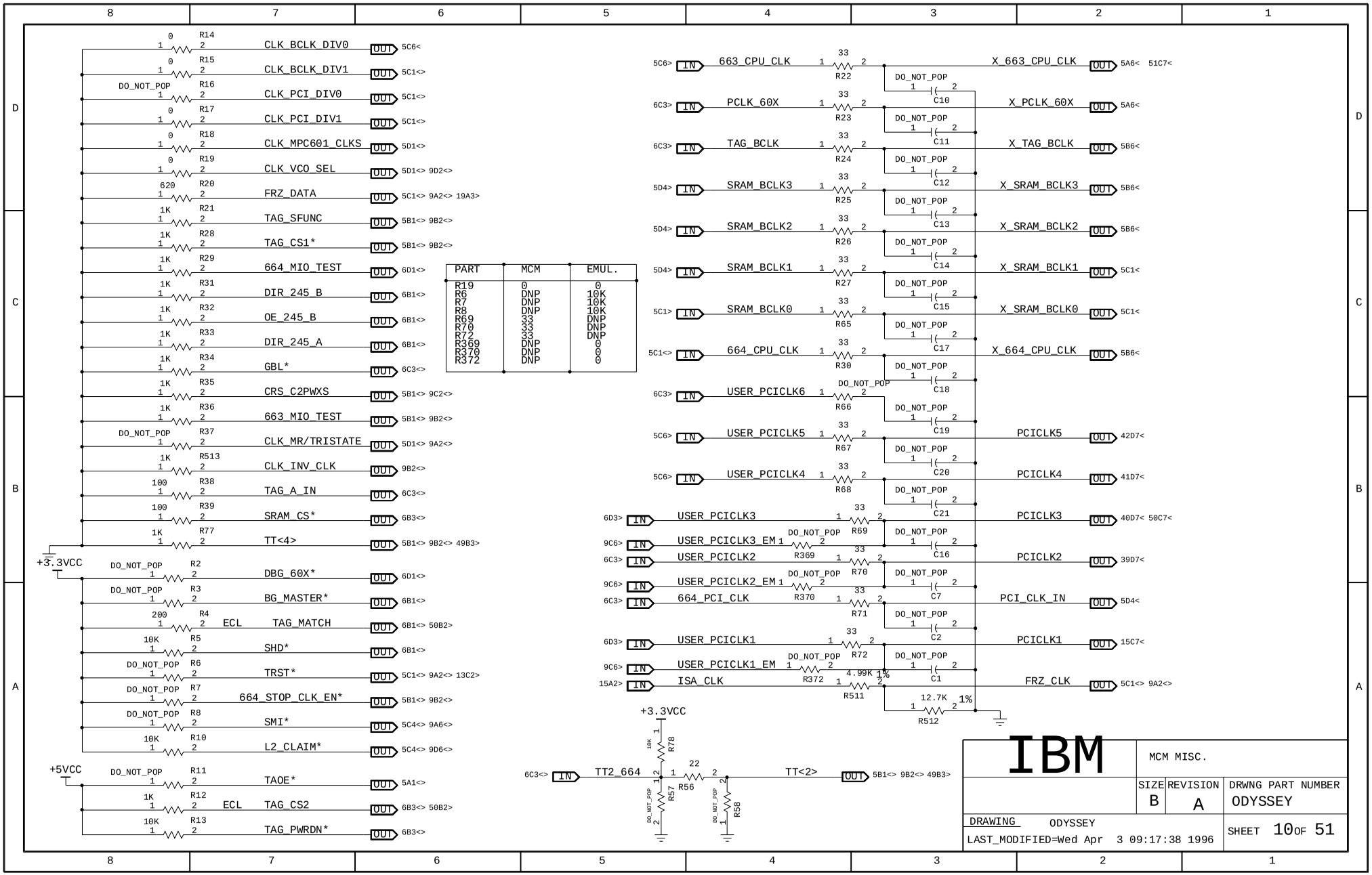
AG30 2
AE28 3
ABUF<28..13>
G26 SRAM_OE*
6B1<>
AB05 13
W08 14
W06 15
W04 16
V05 17
U04 18
T05 19
R04 20
P05 21
N04 22
M05 23
L04 24
AC06 25
AA06 26
V07 27
U06 28
TSIZ<2..0>
R06 2
N06 1
L06 0
J3
PINS
8 OF 18
366
416
C01 USER_PCICLK3
AE01 USER_PCICLK1
J30 664_PCI_CLK
N01 USER_PCICLK2
E33 USER_PCICLK6
E18 PCLK_60X
N30 TAG_BCLK
R08 AACK*
P07 ARTRY*
L08 TS*
K07 XATS*
C12 603E_CSE0*
C14 IT2_664
U10 TBST*
A12 GBL*
M09 CSE
C08 DBB*
AC04 TAG_A_IN
OUT
10B5<
10A5<
10B5<
10B5<
10D5<
10D5<
10A5<
10C6<
10B6<
AB09 0
Y09 1
AC10 2
AA10 3
W10 4
AB11 5
Y11 6
V11 7
DP<7..0>
OUT
R30 ABB*
K21 DBDIS*
B1
G28 0
TC<1..0>
N24 TA_GATES
L24 TAG_WT_DTY_IN
M27 TAG_DATA_11
M31 TAG_PWRDN*
H31 TAG_CS2
L26 TAG_ADDR_13
J26 L2_PD<2>
N28 TAG_TA*
L28 TAG_VLD
J28 TAG_WT
AD29 SRAM_CS*
F03 BR_60X*
D03 BR_664*
P25 TAG_DTY
F11 BG_664*
F09 BG_60X*
6A4>
10A6>
10A6> 50B2>
6A4>
24D7<
10B6>
R171
R170
J3
PINS
9 OF 18
417
473
J04 664_TEST*
G08 DBG_60X*
K05 664_MIO_TEST
H05 0
F07 1
J06 2
G06 3
MEM_BE<3..0>
N12 DUAL_CTRL_REF
L12 ECC_LE_SEL
J12 MEM_RD_SMPL
G12 CPU_RDL_OPEN
AC14 MEM_WRL_OPEN
AA14 C2P_WRL_OPEN
W14 PCI_OL_OPEN
U14 PCI_EXT_SEL
R14 PCI_OUT_SEL
N14 PCI_AD_OE*
L14 MEM_DATA_OE*
J14 CPU_DATA_OE*
G14 603_TEST*
G10
R73
200
C22 L2_PD<1>
AA16 TA*
W16 CKSTP_IN*
U16 INT_60X*
R16 MCP_60X*
N16 DBWO_60X*
L16 TBEN_60X*
J16 TLBISYNC*
G16 RSRV_60X*
AC18 DPE_60X*
AA18 APE_60X*
R18 LSSD_MODE*
N18 L1_TST_CLK*
L18 L2_TST_CLK*
J18 60X_CLK_OUT
G18 603_CPU_PAR_ERR*
G20 603_SBE*
J20 603_MEM_ERR*
K31 TAG_MATCH
N20 BG_MASTER*
D27 SHD*
U20 ROM_LOAD
W20 AOS_RR_MMRS
AA20 TAG_WE*
AC20 TAG_VALID
AC22 TAG_CLEAR*
AA22 SRAM_OE*
W22 SRAM_WE*
U22 SRAM_ALE
R22 SRAM_CNT_EN/ADDR1
N22 SRAM_ADS/ADDR0
L22 DIR_245_B
D29 OE_245_B
G22 DIR_245_A
49B3>
10B6>
10C6>
DO_NOT_POP
C6
49B3>
24D7<
5A1<>
5D1<>
10A6> 50B2>
10A6>
10A6>
6B5<>
10C6>
10C6>
10C6>
STRAPPING FOR 512K L2 CACHE
J1
+5VCC
R43
10K
J7
TAG_DATA_11
TAG_ADDR_13
TAG_ADDR_13
A<13>
TAG_DATA_11
OUT
IN
6A4> 6B3<>
6D5<>
STRAPPING FOR 256K L2 CACHE
IBM
MCM TEST INTERFACE
SIZE B
REVISION A
DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:17:09 1996
SHEET 6 OF 51


PINS 18 OF 18 J3
AC13 AC15 AC17 AC19 AC21 AC23 AC25 AC27 AC29 AC31 AD27 AE03 AE05 AE07 AE09 AE11 AE13 AE15 AE17 AE19 AE21 AE23 AE25 AE26 AE27 AE29 AC16 AE31 AF27 AG03 AG05 AG07 AG09 AG11 AG13 AG15 AG17 AG19 AG21 AG23 AG25 AG26 AG27 AG28 AG29 AG31 AH03 AH27 AJ03 AJ05 AJ07 AJ09 AJ11 AJ13 AJ15 AJ17 AJ19 AJ21 AJ23 AJ25 AJ26 AJ27 AJ28 AJ29 AJ31 AK25 AK27 AK29 AL03 AL05 AL07 AL09 AL11 AL13 AL15 AL17 AL19 AL21 AL23 AL25 AL27 AL29 AL31
PINS 10 OF 18 J3
558
K09 C03 C05 C07 C09 C11 C13 C15 C17 C19 C21 C23 C25 C27 C29 C31 P09 E14 E03 E05 E07 E09 E11 E13 F15 AK01 E17 E19 J08 E21 E23 E25 E27 E29 E31 E16 H09 F13 K25 F17 F19 D21 D23 H21 R10 H23 AC12 H15 G03 G05 G07 G09 G11 G13 G15 G17 G19 G21 G23 G24 G25 J10 G27 J22 G29 P23 G31 H11 H13 J15 H19 K15 B23 H25 M07 N08
PINS 11 OF 17 J3
H17 J24 AA08 T07 J03 J05 J07 J09 J11 J13 J17 J19 J21 J23 J25 J27 J29 J31 K11 K13 K17 K19 H07 K23 J02 AA12 L20 L03 L05 L07 L09 L11 L13 L15 L17 L19 L21 L23 L25 L27 L29 L31 M11 M13 M15 M17 M19 M21 M23 M25 U08 M29 AA26 N03 N05 N07 N09 N11 N13 N15 N17 N19 N21 N23 N25 N27 N29 N31 P11 P13 P15 P17 P19 P21 E20 R20 R03 R05
PINS 12 OF 17 J3
728
R07 R09 R11 R12 R13 R21 R23 R25 R27 R29 R31 T09 T11 T13 T15 T17 T19 T21 Y07 U03 U05 U07 U09 U11 U12 U13 U18 U21 U23 U25 U27 U29 U31 V09 V13 V15 V17 V19 V21 C06 W03 W05 W07 W09 W11 W12 W13 W18 W21 W23 W25 W27 W29 W31 Y13 Y15 Y17 Y19 Y21 Y23 AA03 AA05 AA07 AA09 AA11 AA13 AA15 AA17 AA19 AA21 AA23 AA25 AA27 AA29 AA31 AB13 AB15 AB17 AB19 AB21 AB23 AC03 AC05 AC07 AC09 AC11
PINS 13 OF 17 J3
813
B04 B08 B12 B16 B18 B22 B26 B30 D02 D06 D10 D14 D20 D24 D28 D32 F04 F08 F12 F16 F18 F22 F26 F30 H02 H06 H10 H14 H20 H24 H28 H32 K04 K08 K12 K16 K18 K22 K26 K30 M02 M06 M10 M14 M20 M24 M28 M32 P04 P08 P12 P16 P18 P22 P26 P30 T02 T06 T10 T14 T20 T24 T28 T32
876
PINS 14 OF 17 J3
877
V02 V06 V10 V14 V20 V24 V28 V32 Y04 Y08 Y12 Y16 Y18 Y22 Y26 Y30 AB02 AB06 AB10 AB14 AB20 AB24 AB28 AB32 AD04 AD08 AD12 AD16 AD18 AD22 AD26 AD30 AF02 AF06 AF10 AF14 AF20 AF24 AF28 AF32 AH04 AH08 AH12 AH16 AH18 AH22 AH26 AH30 AK02 AK06 AK10 AK14 AK20 AK24 AK28 AK32 AM04 AM08 AM12 AM16 AM18 AM22 AM26 AM30
940
PINS 15 OF 17 J3
941
+3.3VCC
B02 60X_AVDD
BI
49B6>
B06 B24 B28 B32 D04 D26 D30 F02 F06 F24 F28 F32 H04 H26 H30 K02 K06 K24 K28 K32 M04 P02 P06 P10 P14 P20 P24 P28 P32 R15 R17 R19 T04 T08 T12 T16 T18 U15 U17 U19 V04 V08 V12 V16 V18 W15 W17 W19 Y02 Y06 Y10 Y14 Y20 Y24
995
PINS 16 OF 17 J3
996
SRAM_PWR
BI
8C6<>
8D8<>
Y28 Y32 AB04 AB08 AB12 AB16 AB18 AB22 AB26 AB30 AD02 AD06 AD10 AD14 AD20 AD24 AD28 AD32 AF04 AF08 AF12 AF16 AF18 AF22 AF26 AF30 AH02 AH06 AH10 AH14 AH20 AH24 AH28 AH32 AK04 AK08 AK12 AK16 AK18 AK22 AK26 AK30 AM02 AM06 AM10 AM14 AM20 AM24 AM28 AM32
1045
PINS 17 OF 18 J3
+3.3VCC
B10 B14 B20 D08 D12 D16 D18 D22 F10 F14 F20 H08 H12 H16 H18 H22 K10 K14 K20 M08 M12 M16 M18
+5VCC
M22 M26 M30 T22 T26 T30 V22 V26 V30
+3.3VCC
+5VCC
J17 J18
1 2 3
1 2 3
SRAM_PWR
X1
MECH PART
JUMPER1X2
X4
MECH PART
JUMPER1X2
12MIL
NOTE: THESE 1X3 HEADERS TO BE PLACED SIDE BY SIDE. 2X2 JUMPER TO BE INSTALLED SUCH THAT EITHER +3.3V OR +5V IS TIED TO SRAM_PWR.
+5VCC
C202 C203 C204 C205 C207 C206 C208 C209 C210
+3.3VCC
C211 C212 C213 C214 C215
33UF
0.01UF
IBM
MCM INTERFACE (POWER)
SIZE B
REVISION A
DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:17:23 1996
SHEET 7 OF 51


J36
CONNBERG2X36
DO_NOT_POP
+3.3VCC
SRAM_PWR
8C6<> 7D2<>
BI
MD<63..0>
BI
5D7<> 8B3<> 37B2<> 37B8<> 38B2<> 38B8<>
J37
CONNBERG2X36
DO_NOT_POP
MA<11..0>
OUT
5B6> 37B7< 38B7<
8D8<> 7D2<>
BI
SRAM_PWR
MCE<7..0>*
OUT
5B6> 37C2< 37C7< 38C2< 38C7<
MDP<7..0>
BI
5B6> 37A2<> 37A8<> 38A2<> 38A8<>
+3.3VCC
MD<63..0>
BI
5D7<> 8D5<> 37B2<> 37B8<> 38B2<> 38B8<>
+5VCC
C216 C217 C218 C219 C220
33UF
0.01UF
C221 C222 C223 C224 C225
+3.3VCC
33UF
0.01UF
MRE<3..0>*
OUT
5C6> 37D7< 38D7<
IBM
EMULATOR INTERFACE
DRAM BUS & CLOCKS
SIZE
B
REVISION
A
DRWNG PART NUMBER
ODYSSEY
DRAWING
ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:17:31 1996
SHEET 8 OF 51



IBM	EMULATOR INTERFACE PCI BUS & MISC. CNTL		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:17:34 1996	SHEET 9 OF 51		


CLK_BCLK_DIV0
CLK_BCLK_DIV1
CLK_PCI_DIV0
CLK_PCI_DIV1
CLK_MPC601_CLKS
CLK_VCO_SEL
FRZ_DATA
TAG_SFUNC
TAG_CS1*
664_MIO_TEST
DIR_245_B
OE_245_B
DIR_245_A
GBL*
CRS_C2PWXS
663_MIO_TEST
CLK_MR/TRISTATE
CLK_INV_CLK
TAG_A_IN
SRAM_CS*
TT<4>
+3.3VCC
DBG_60X*
BG_MASTER*
TAG_MATCH
SHD*
TRST*
664_STOP_CLK_EN*
SMI*
L2_CLAIM*
+5VCC
TAOE*
TAG_CS2
TAG_PWRDN*
663_CPU_CLK
PCLK_60X
TAG_BCLK
SRAM_BCLK3
SRAM_BCLK2
SRAM_BCLK1
SRAM_BCLK0
664_CPU_CLK
USER_PCICLK6
USER_PCICLK5
USER_PCICLK4
USER_PCICLK3
USER_PCICLK3_EM
USER_PCICLK2
USER_PCICLK2_EM
664_PCI_CLK
USER_PCICLK1
USER_PCICLK1_EM
ISA_CLK
X_663_CPU_CLK
X_PCLK_60X
X_TAG_BCLK
X_SRAM_BCLK3
X_SRAM_BCLK2
X_SRAM_BCLK1
X_SRAM_BCLK0
X_664_CPU_CLK
PCICLK5
PCICLK4
PCICLK3
PCICLK2
PCI_CLK_IN
PCICLK1
FRZ_CLK
TT2_664
TT<2>
PART MCM EMUL.
R19 0 0
R6 DNP 10K
R7 DNP 10K
R8 DNP 10K
R69 33 DNP
R70 33 DNP
R72 33 DNP
R369 DNP 0
R370 DNP 0
R372 DNP 0
IBM
MCM MISC.
SIZE B
REVISION A
DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:17:38 1996
SHEET 10 OF 51

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IBM	BLANK		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Mon Jan 29 16:02:20 1996	SHEET 11 OF 51		

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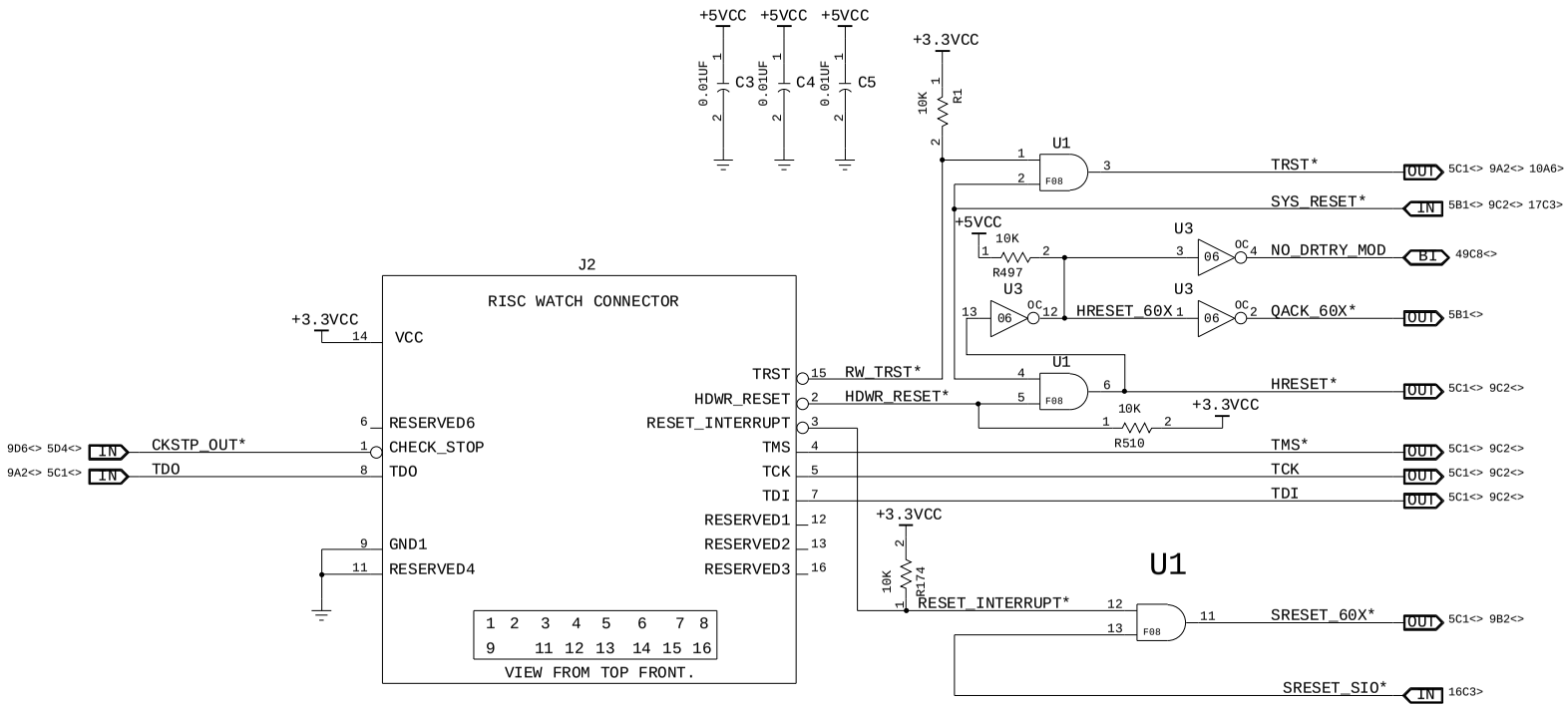
IBM	BLANK		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Mon Jan 29 16:02:35 1996	SHEET 12 OF 51		



IBM	RISCWATCH CONNECTOR		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:17:46 1996	SHEET 13 OF 51		

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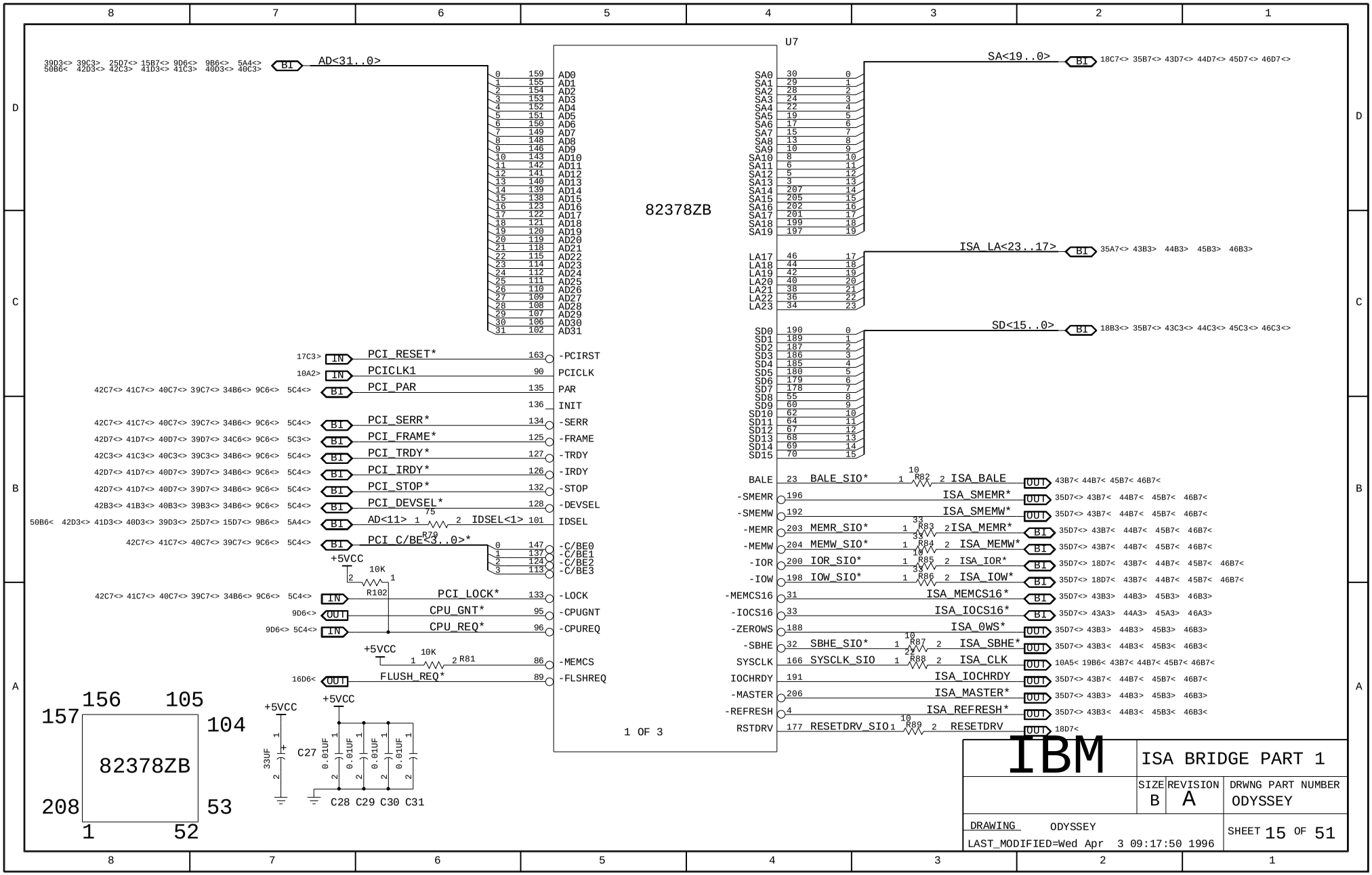
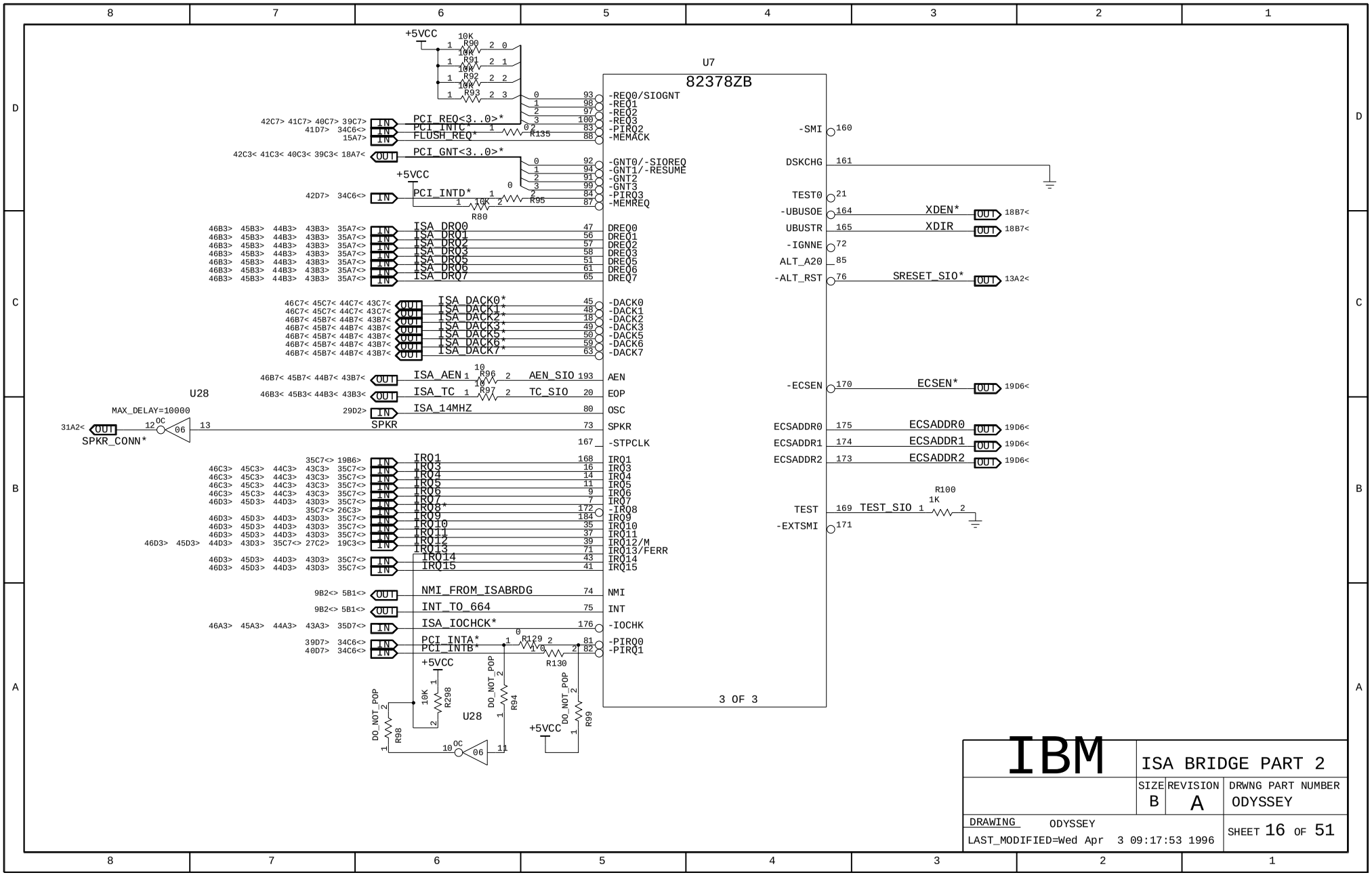
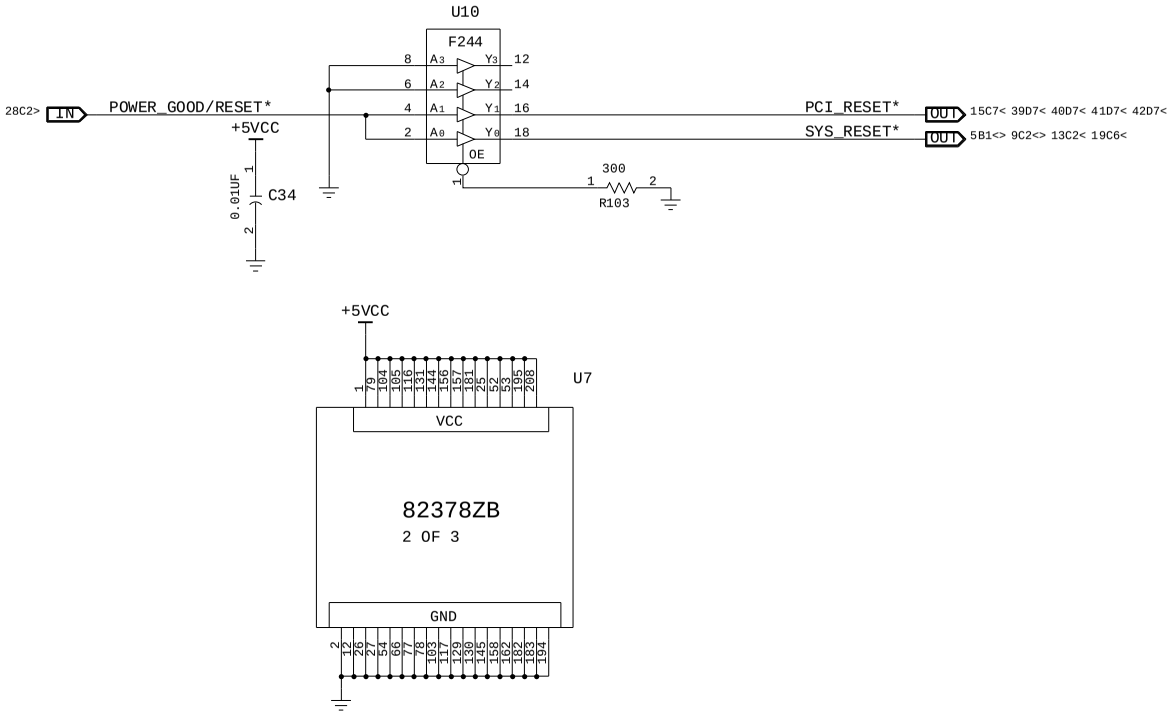
IBM	BLANK		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Mon Jan 29 16:02:54 1996			SHEET 14 OF 51



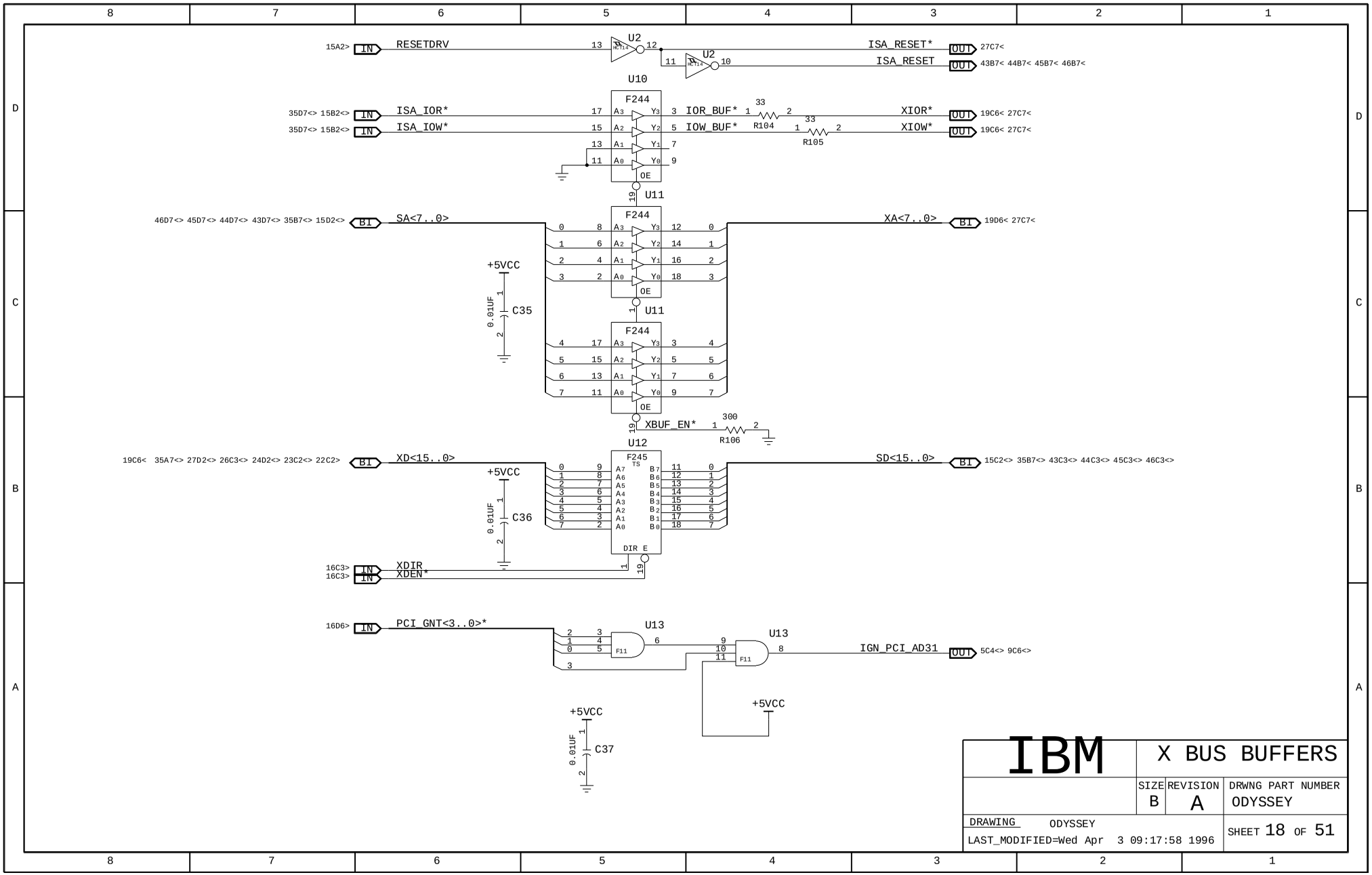
IBM	ISA BRIDGE PART 1	
	SIZE B / REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:17:50 1996		SHEET 15 OF 51



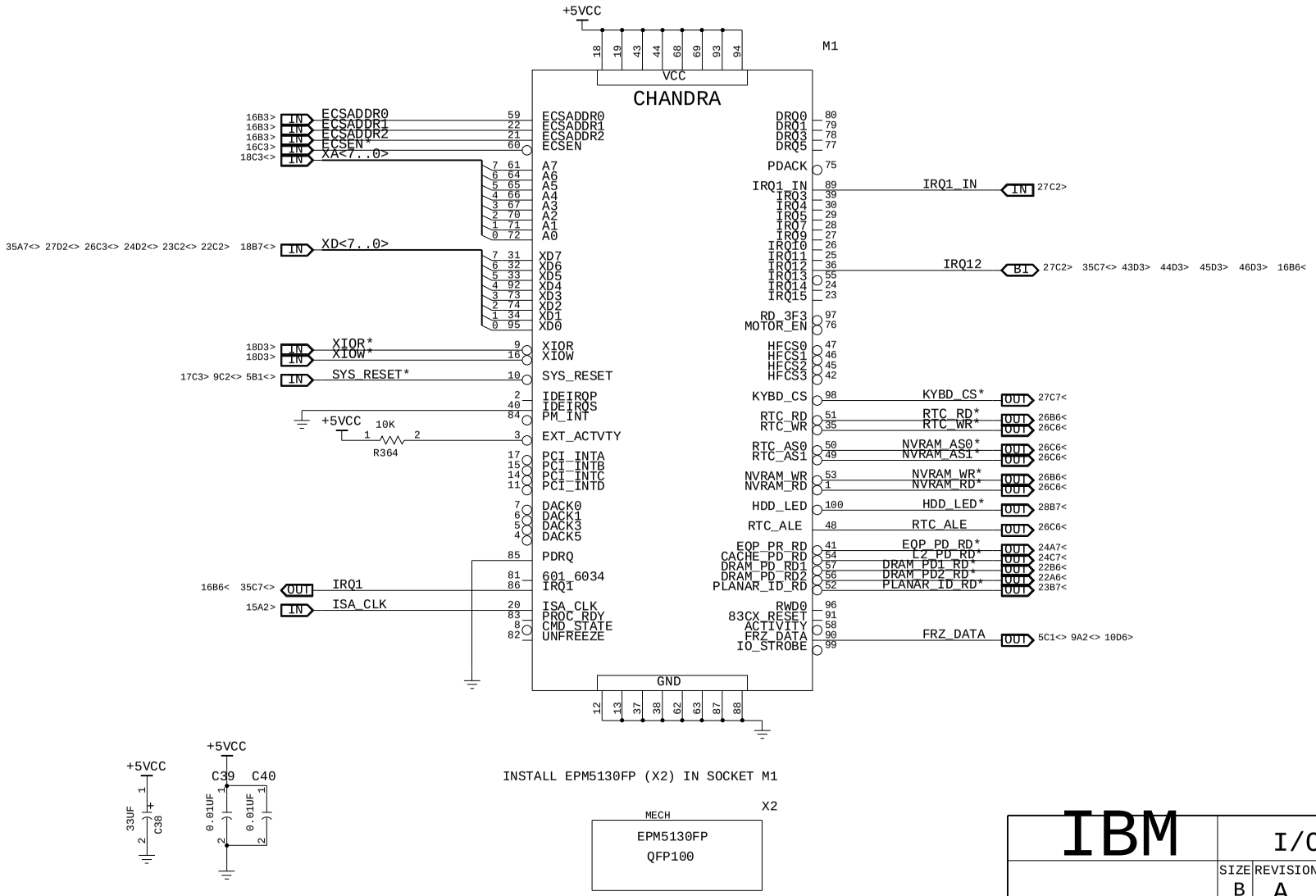
IBM	ISA BRIDGE PART 2		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:17:53 1996	SHEET 16 OF 51		



IBM	ISA BRIDGE PART 3		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:17:56 1996	SHEET 17 OF 51		



IBM	X BUS BUFFERS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:17:58 1996	SHEET 18 OF 51		

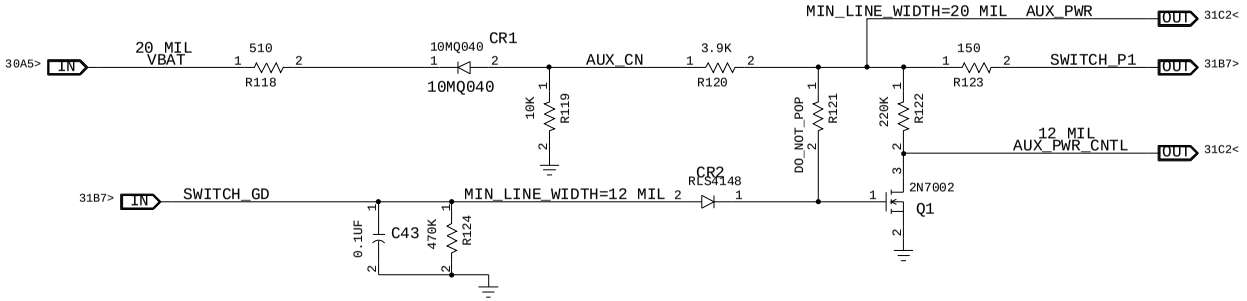


IBM	I/O EPLD		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY			SHEET 19 OF 51
LAST_MODIFIED=Wed Apr 3 09:18:01 1996			

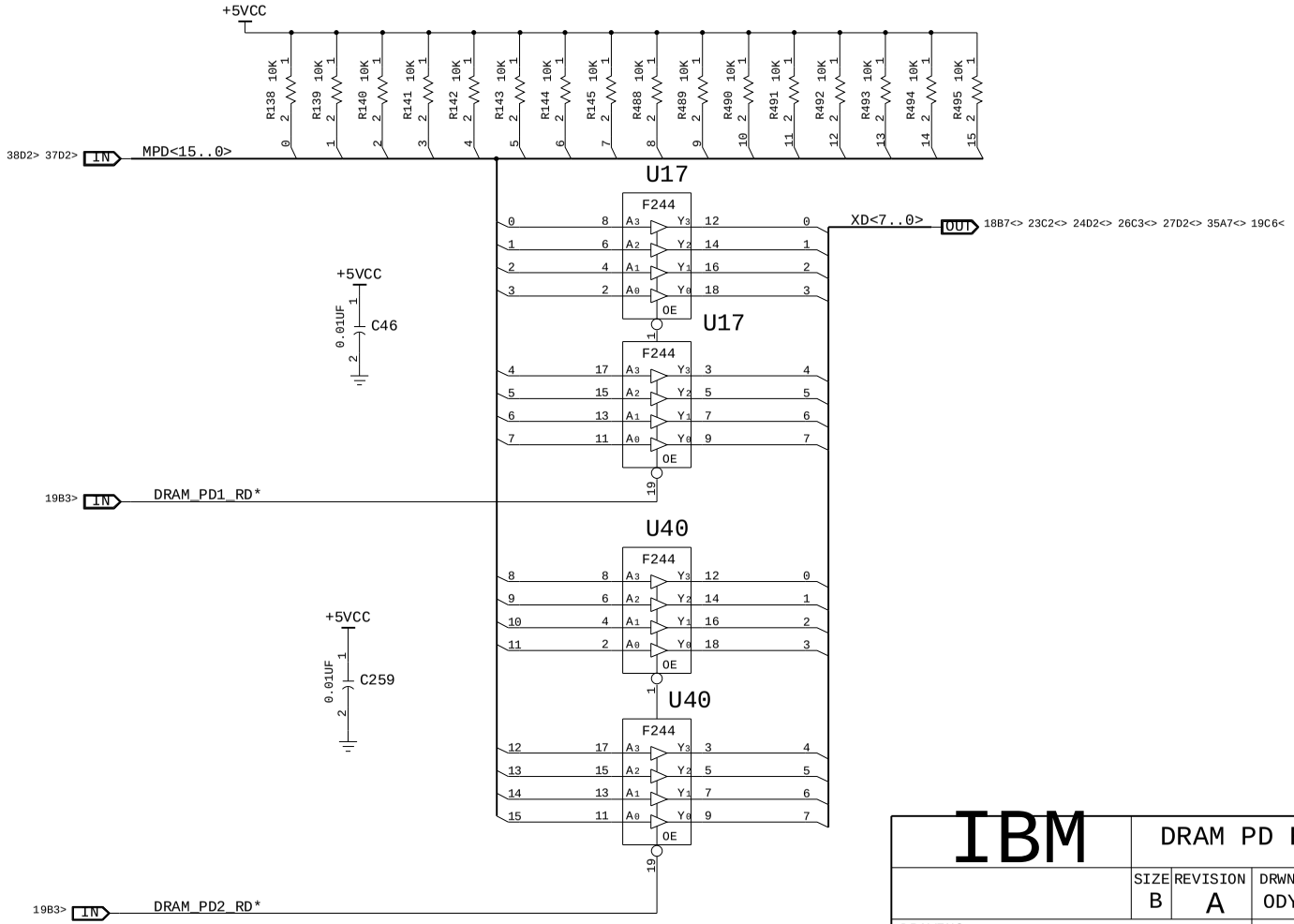
BLANK

IBM

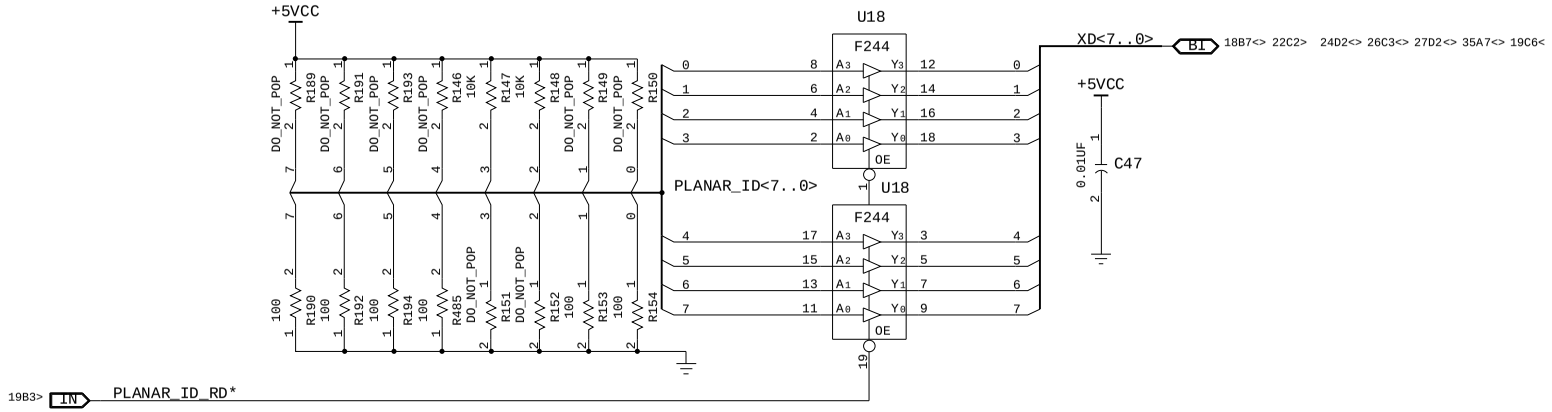
BLANK			
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Mon Jan 29 16:03:50 1996			SHEET 20 OF 51



IBM	POWER SUPPLY MISC.		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY ODY LAST_MODIFIED=Wed Apr 3 09:18:03 1996	SHEET 21 OF 51		



IBM	DRAM PD RD. BUF.		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY ODY LAST_MODIFIED=Wed Apr 3 09:18:06 1996	SHEET 22 OF 51		



IBM

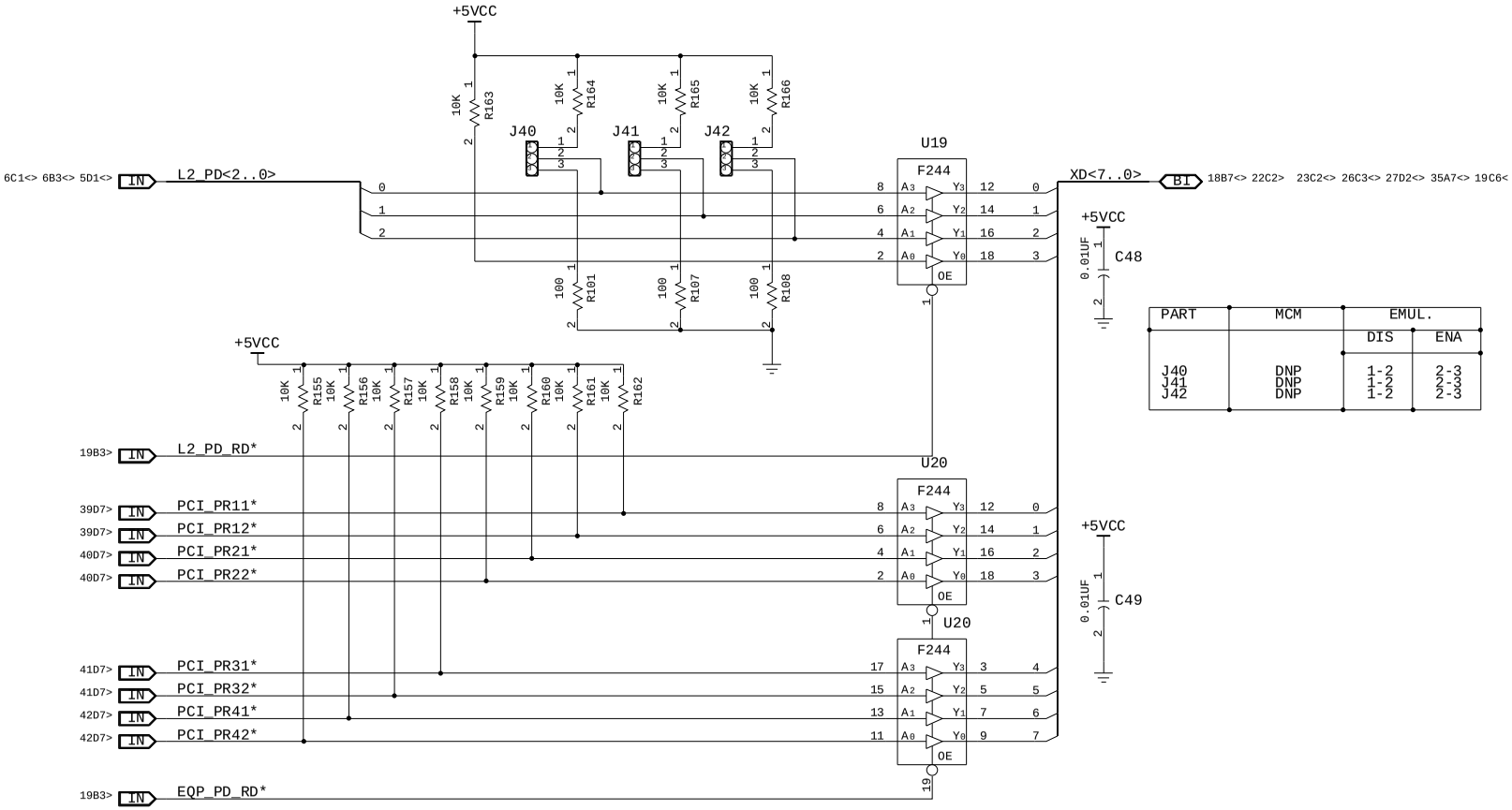
PLANAR ID RD.

SIZE	REVISION	DRWNG PART NUMBER
B	A	ODYSSEY

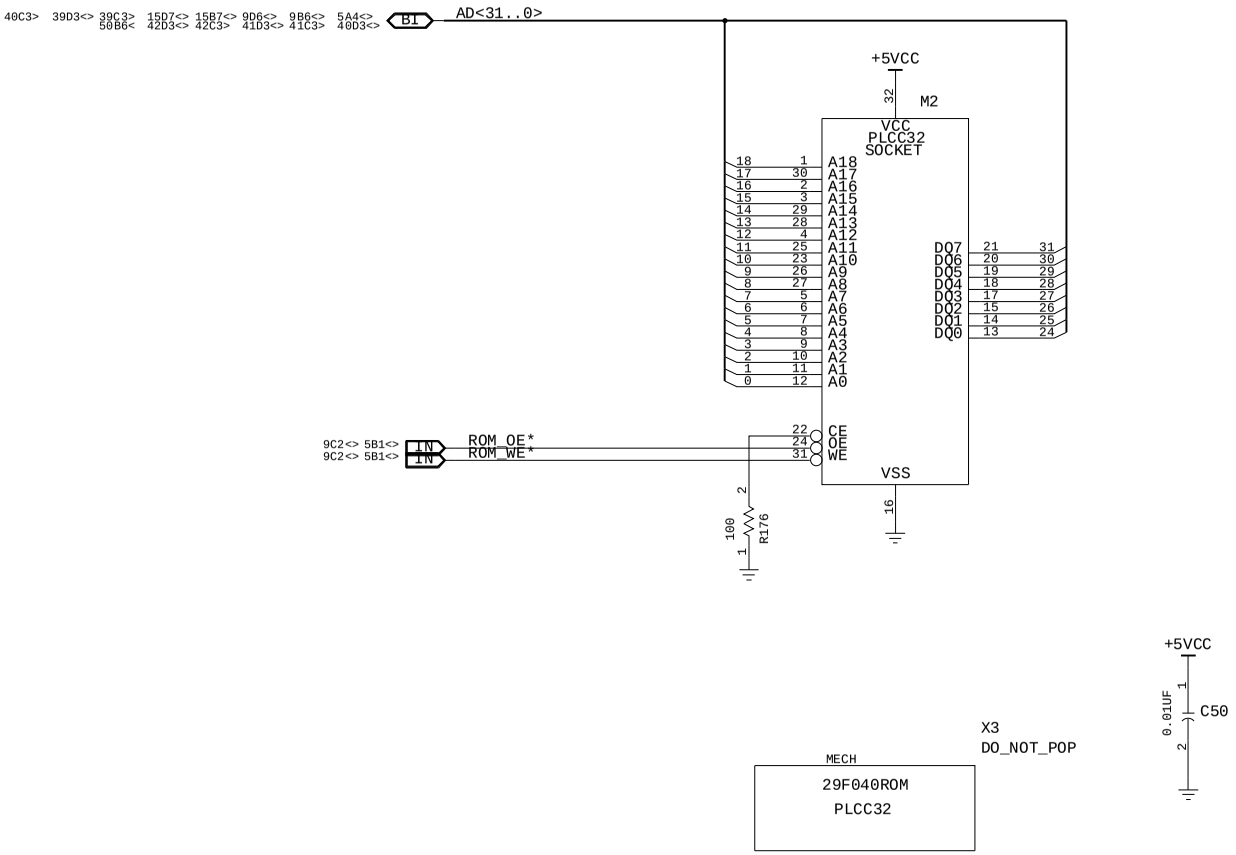
DRAWING ODYSSEY

LAST_MODIFIED=Wed Apr 3 09:18:08 1996

SHEET 23 OF 51

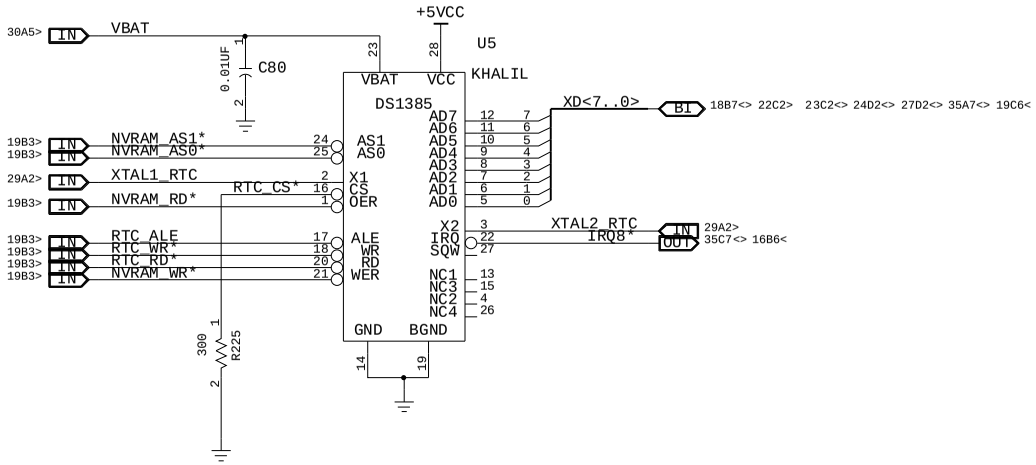


IBM	L2 & EQP. PRESENCE RD. BUF.		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:11 1996	SHEET 24 OF 51		

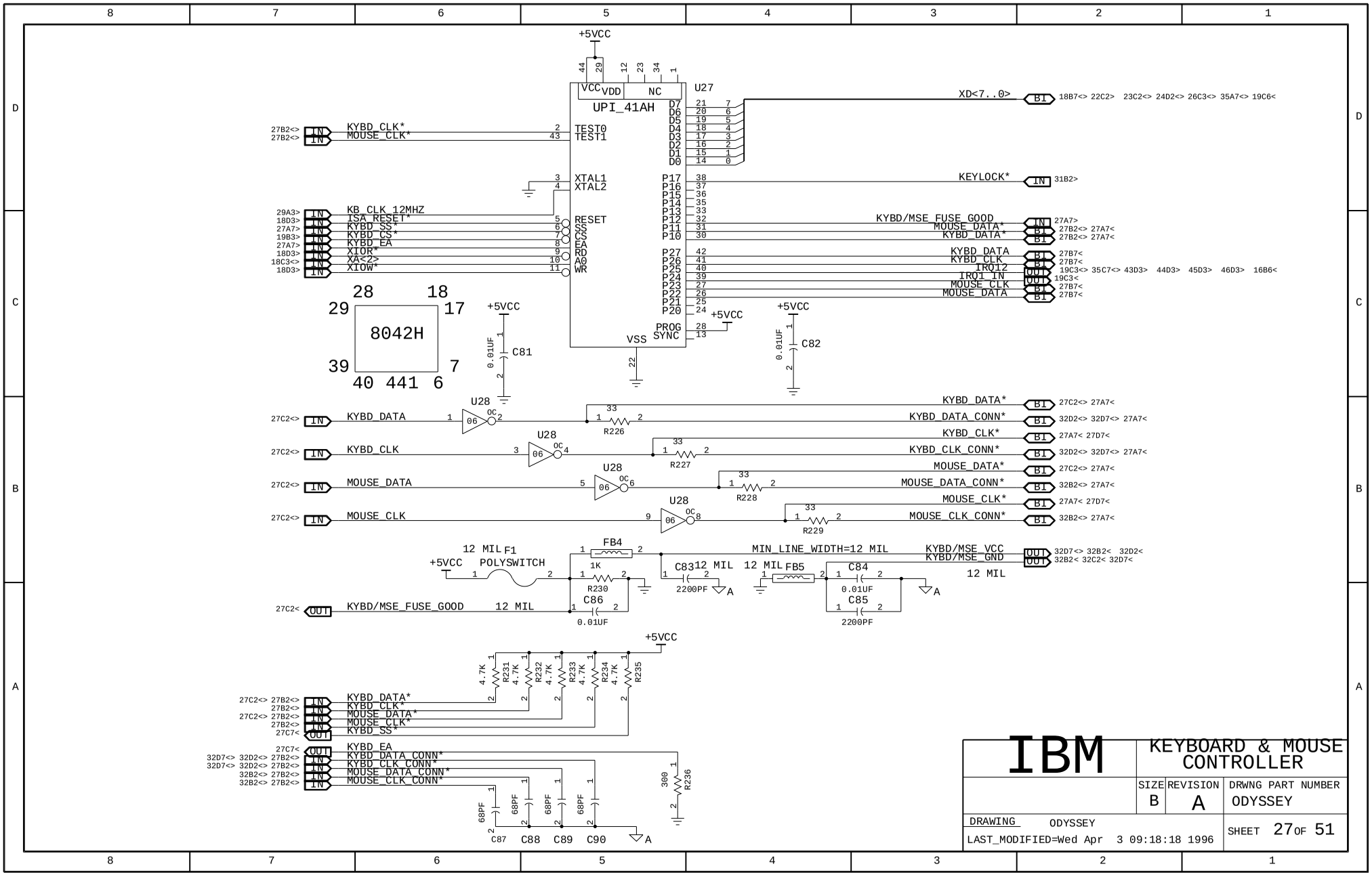


PLACE X3 INTO M2 SOCKET

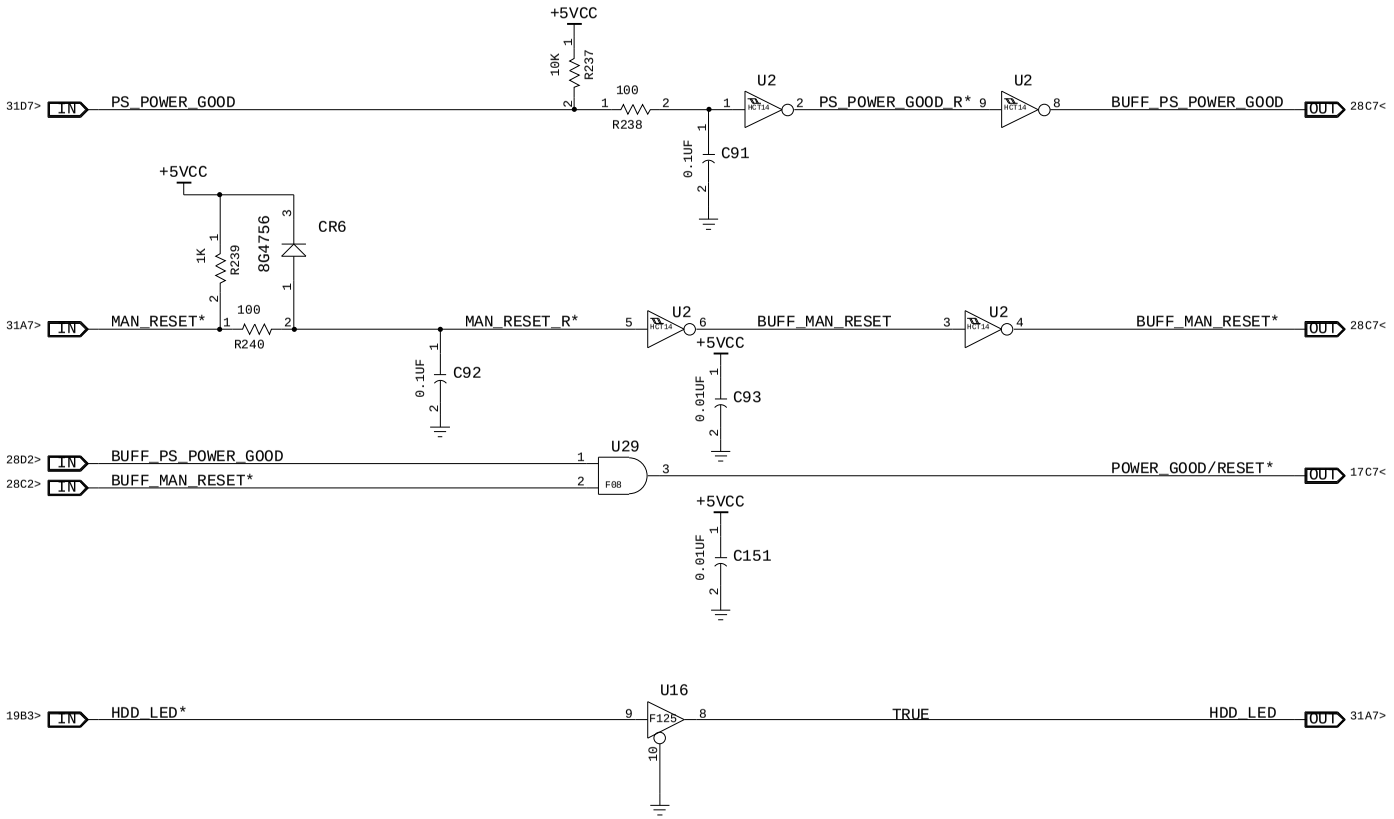
IBM	ROM & ROM SOCKET		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:13 1996	SHEET 25 OF 51		



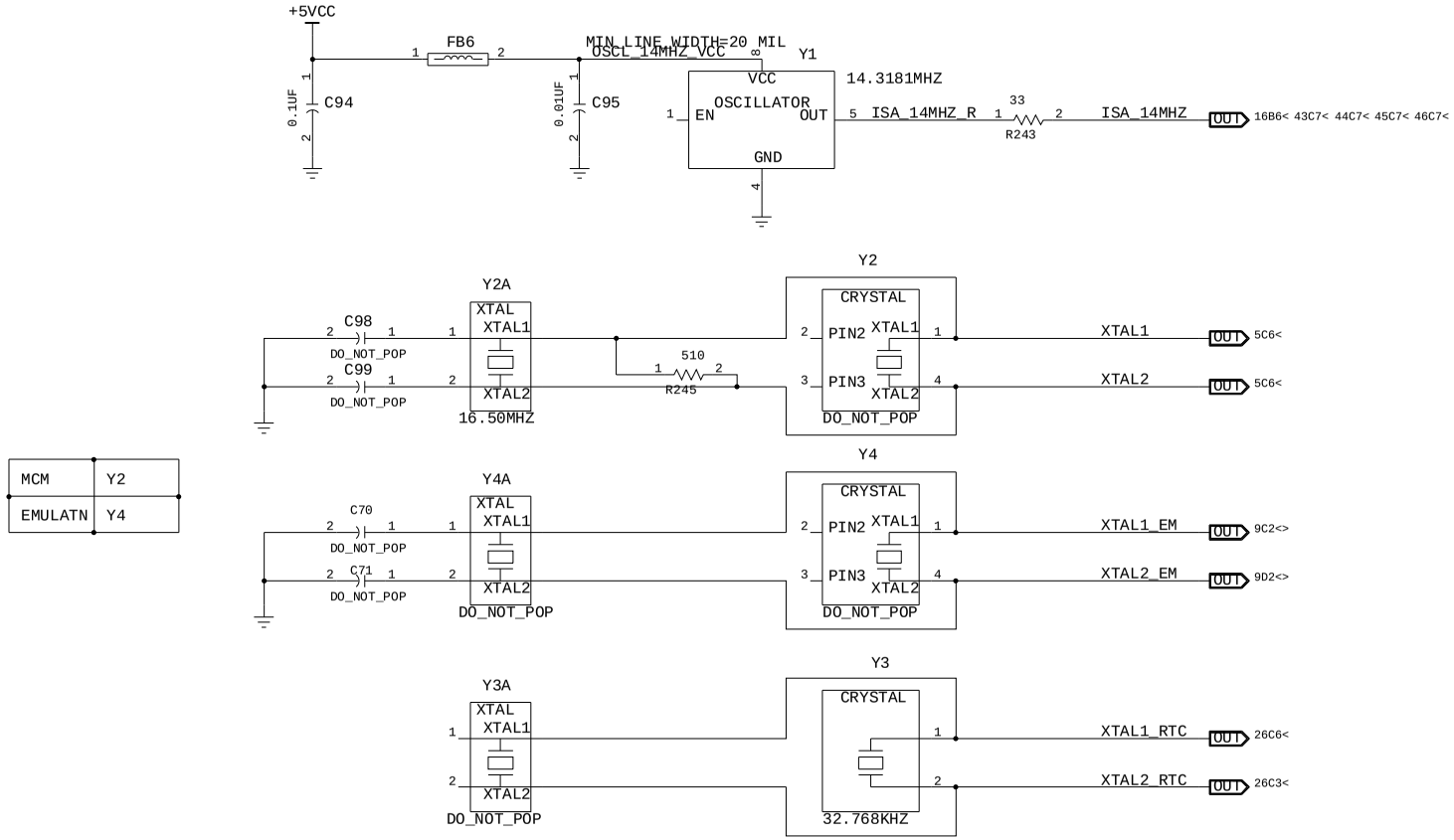
IBM	REAL TIME CLOCK		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:15 1996	SHEET 26 OF 51		



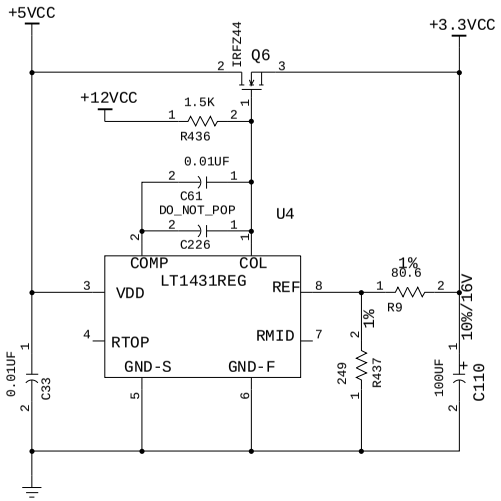
IBM	KEYBOARD & MOUSE CONTROLLER		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY			SHEET 27 OF 51
LAST_MODIFIED=Wed Apr 3 09:18:18 1996			

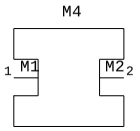


IBM	FRONT PANEL CKT.		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:21 1996	SHEET 28 OF 51		



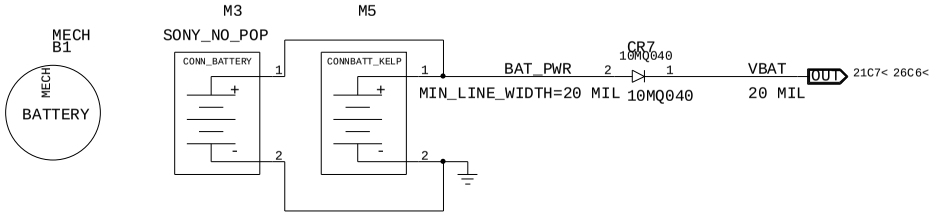
IBM	CLOCKS CKT		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:23 1996	SHEET 29 OF 51		



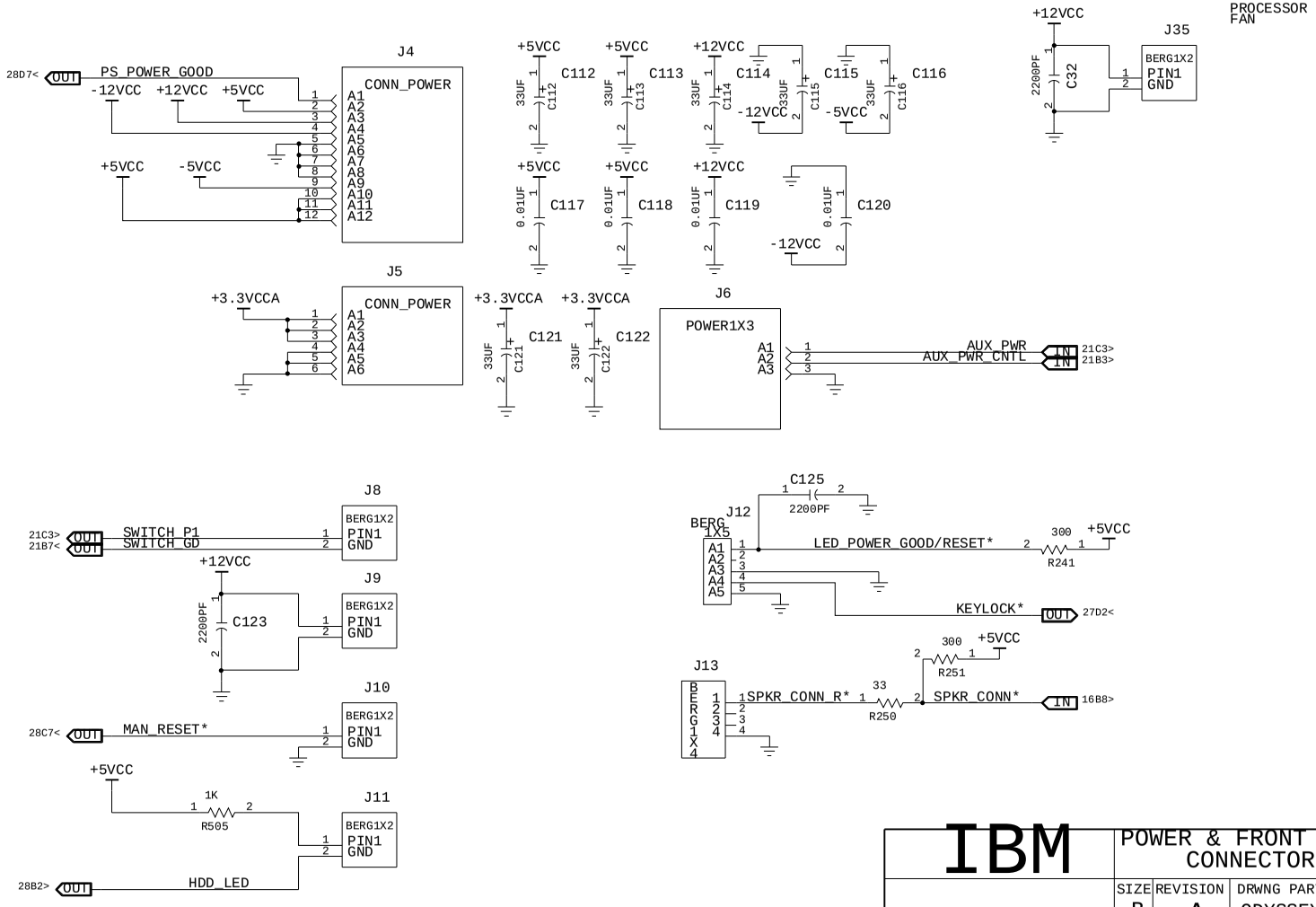


NOTE: VOLTAGE REGULATOR OUTPUT CAN BE VARRIED BY CHANGING R9.

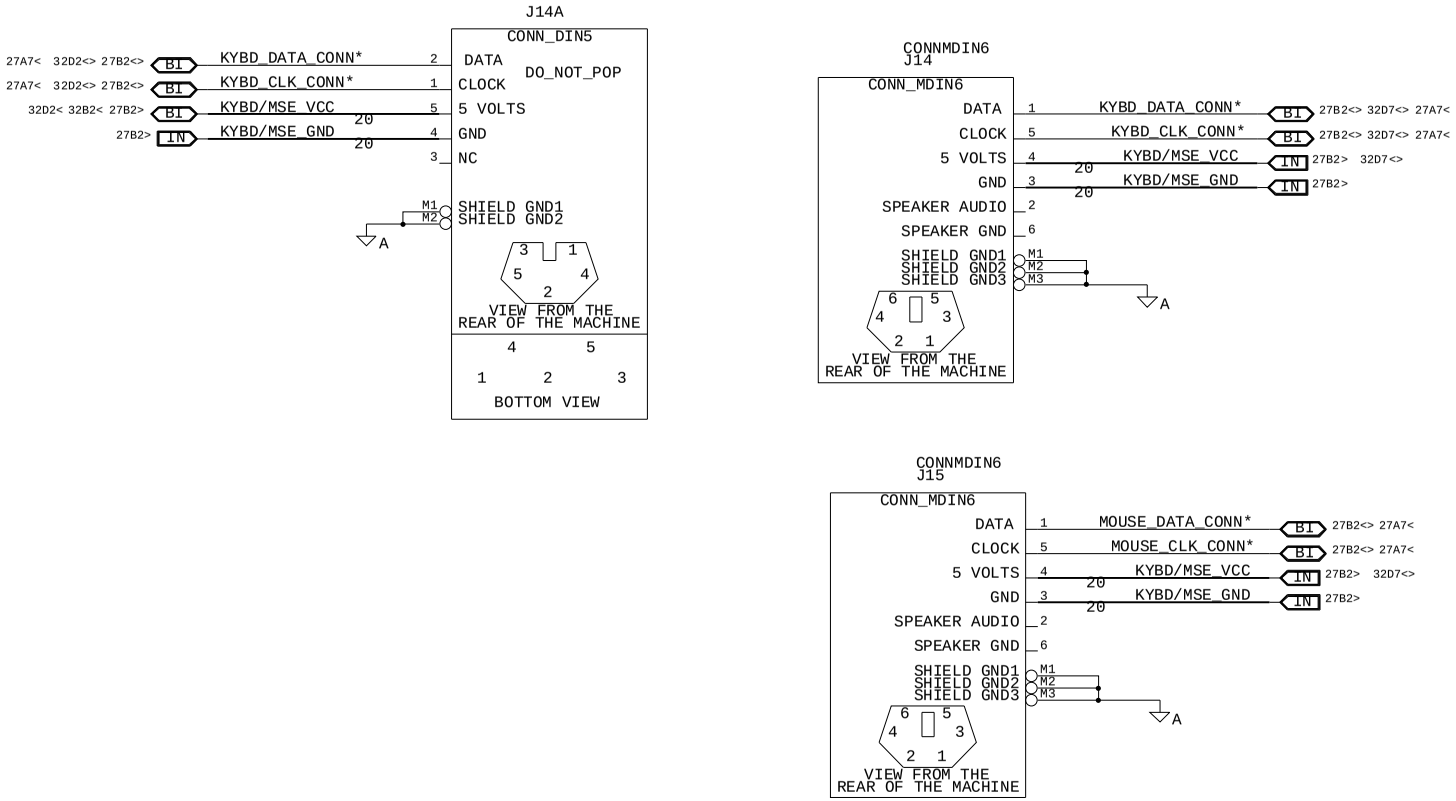
VOLATGE	R9
2.5V	DO_NOT_POP
3.3V	80.6 1%
3.6V	110 1%



IBM	VOLTAGE REGULATORS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY ODY LAST_MODIFIED=Wed Apr 3 09:18:25 1996	SHEET 30 OF 51		



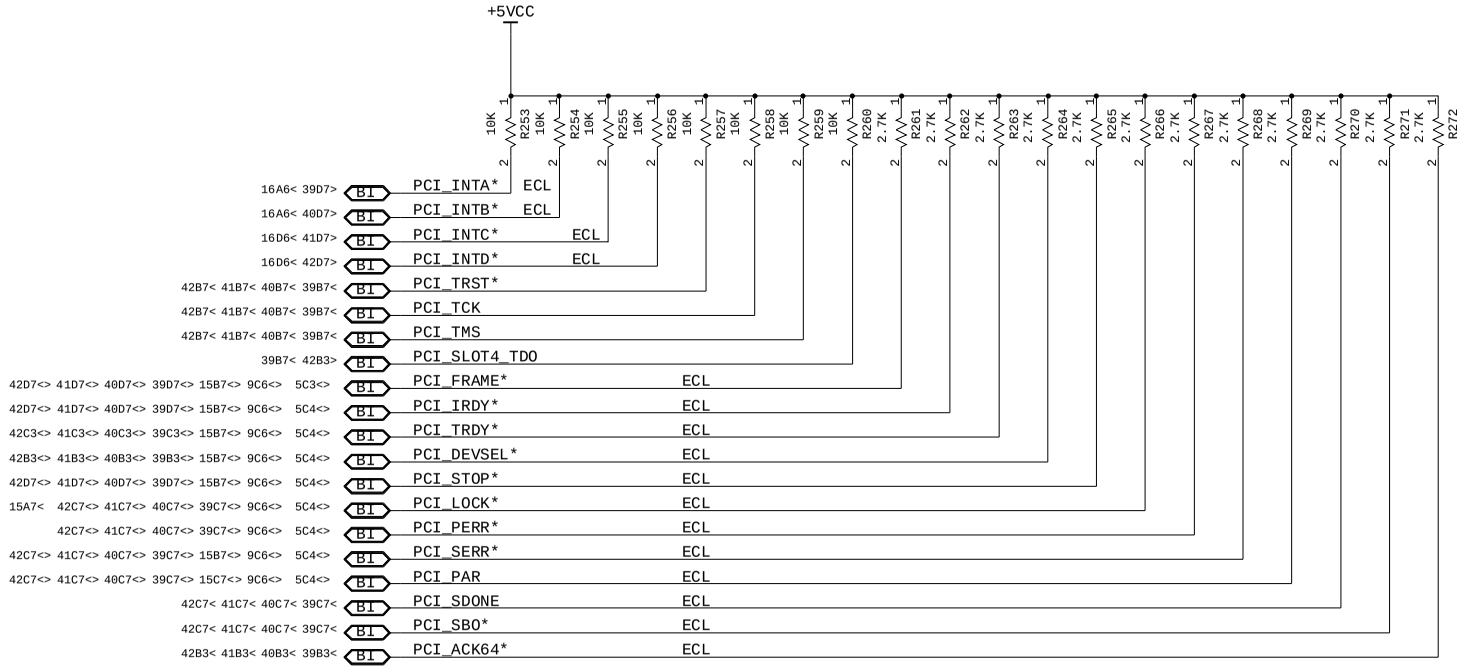
IBM	POWER & FRONT PANEL CONNECTORS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:28 1996			SHEET 31 OF 51



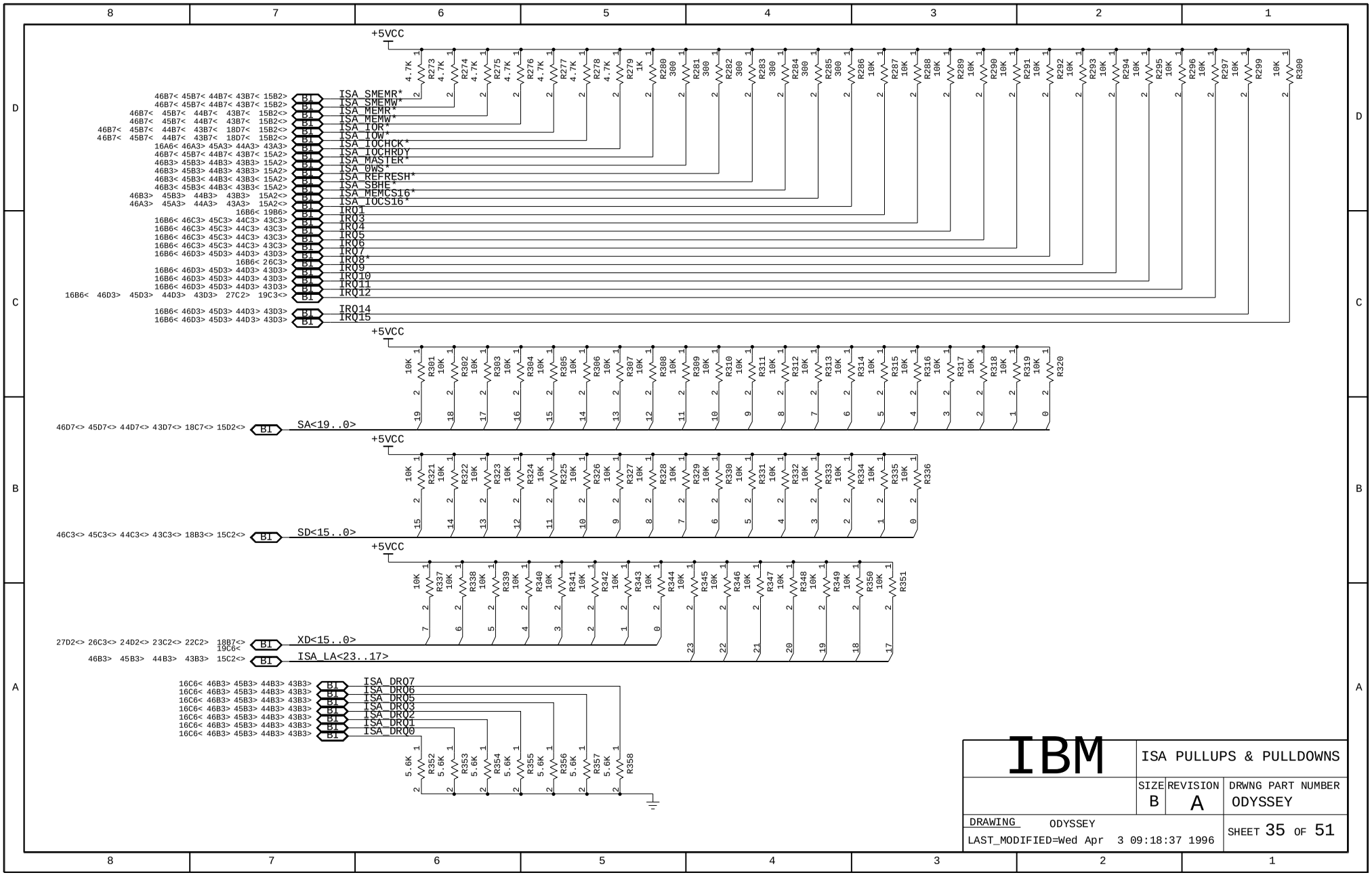
IBM	KEYBOARD & MOUSE CONNECTORS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:31 1996	SHEET 32 OF 51		

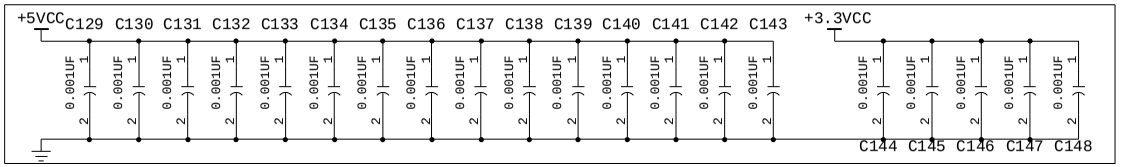
BLANK

IBM	BLANK		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Mon Jan 29 16:04:21 1996	SHEET 33 OF 51		

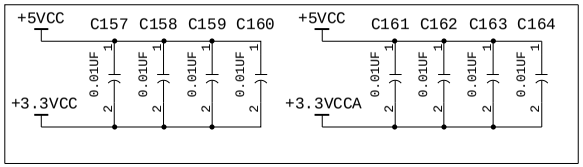


IBM	PCI PULLUPS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:32 1996	SHEET 34 OF 51		

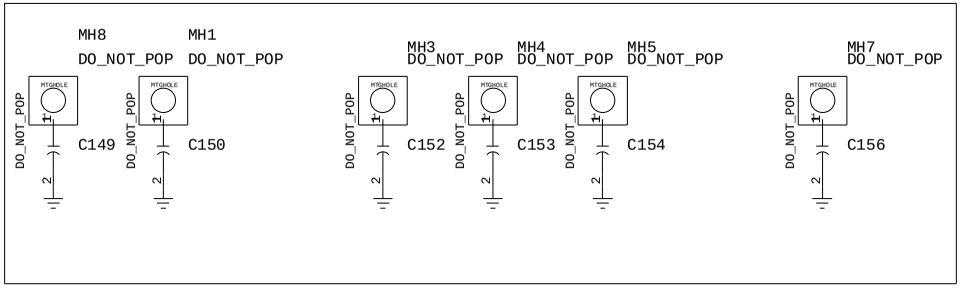

+5VCC
R273 4.7K
R274 4.7K
R275 4.7K
R276 4.7K
R277 4.7K
R278 4.7K
R279 1K
R280 300
R281 300
R282 300
R283 300
R284 300
R285 300
R286 10K
R287 10K
R288 10K
R289 10K
R290 10K
R291 10K
R292 10K
R293 10K
R294 10K
R295 10K
R296 10K
R297 10K
R299 10K
R300 10K
ISA_SMEMR*
ISA_SMEMW*
ISA_MEMR*
ISA_MEMW*
ISA_IOR*
ISA_IOW*
ISA_IOCHCK*
ISA_IOCHRDY
ISA_MASTER*
ISA_0WS*
ISA_REFRESH*
ISA_SBHE*
ISA_MEMCS16*
ISA_IOCS16*
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8*
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
+5VCC
R301 10K
R302 10K
R303 10K
R304 10K
R305 10K
R306 10K
R307 10K
R308 10K
R309 10K
R310 10K
R311 10K
R312 10K
R313 10K
R314 10K
R315 10K
R316 10K
R317 10K
R318 10K
R319 10K
R320 10K
SA<19..0>
+5VCC
R321 10K
R322 10K
R323 10K
R324 10K
R325 10K
R326 10K
R327 10K
R328 10K
R329 10K
R330 10K
R331 10K
R332 10K
R333 10K
R334 10K
R335 10K
R336 10K
SD<15..0>
+5VCC
R337 10K
R338 10K
R339 10K
R340 10K
R341 10K
R342 10K
R343 10K
R344 10K
R345 10K
R346 10K
R347 10K
R348 10K
R349 10K
R350 10K
R351 10K
XD<15..0>
ISA_LA<23..17>
ISA_DRQ7
ISA_DRQ6
ISA_DRQ5
ISA_DRQ3
ISA_DRQ2
ISA_DRQ1
ISA_DRQ0
R352 5.6K
R353 5.6K
R354 5.6K
R355 5.6K
R356 5.6K
R357 5.6K
R358 5.6K
IBM
ISA PULLUPS & PULLDOWNS
SIZE B
REVISION A
DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:18:37 1996
SHEET 35 OF 51



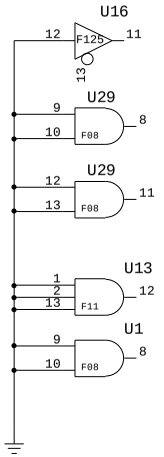
EMC CAPACITORS (PLACED ON THE EDGES OF THE CARD)



BRIDGING CAPACITORS

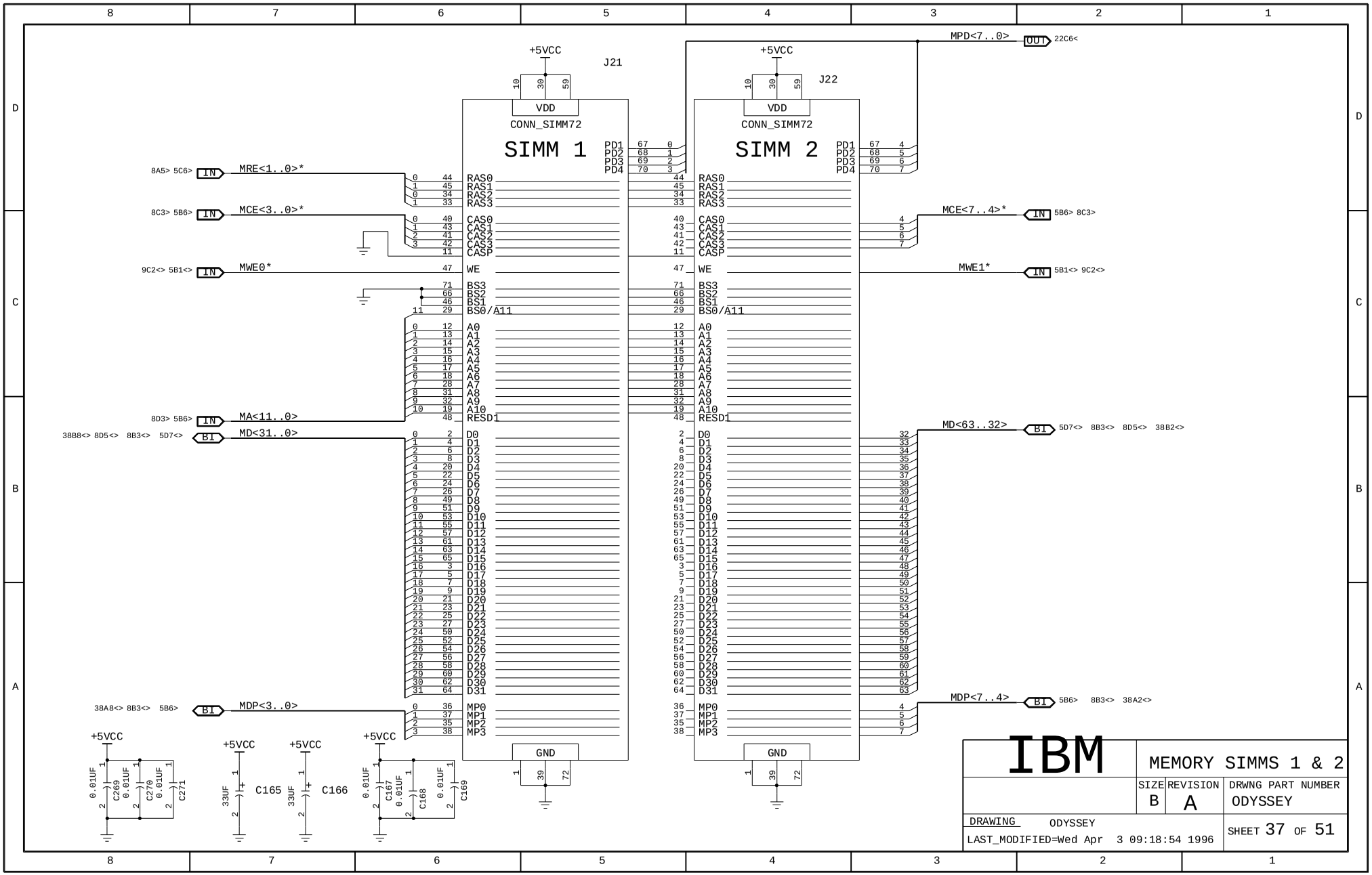


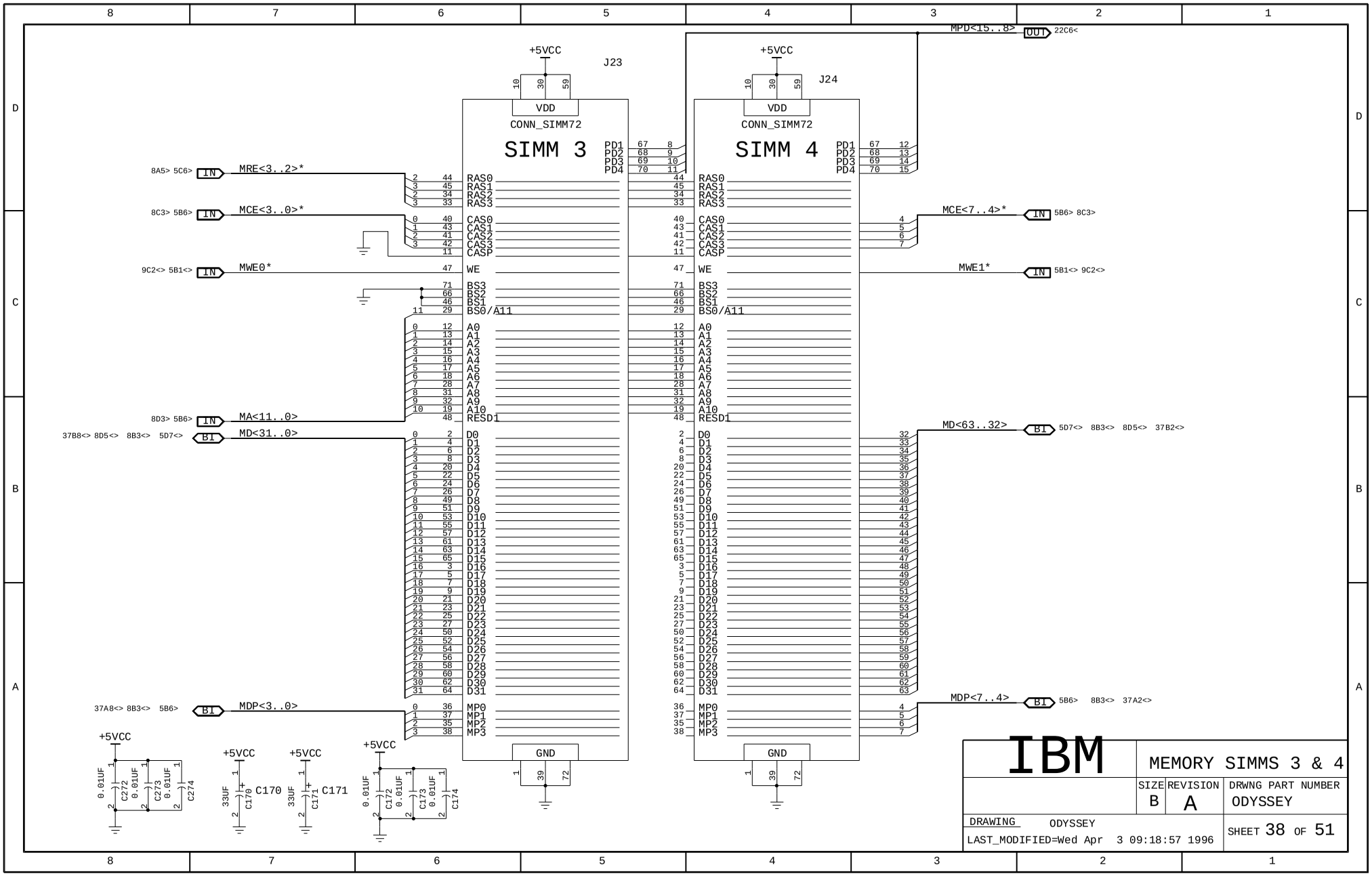
EMC MOUNTING HOLE CAPACITORS

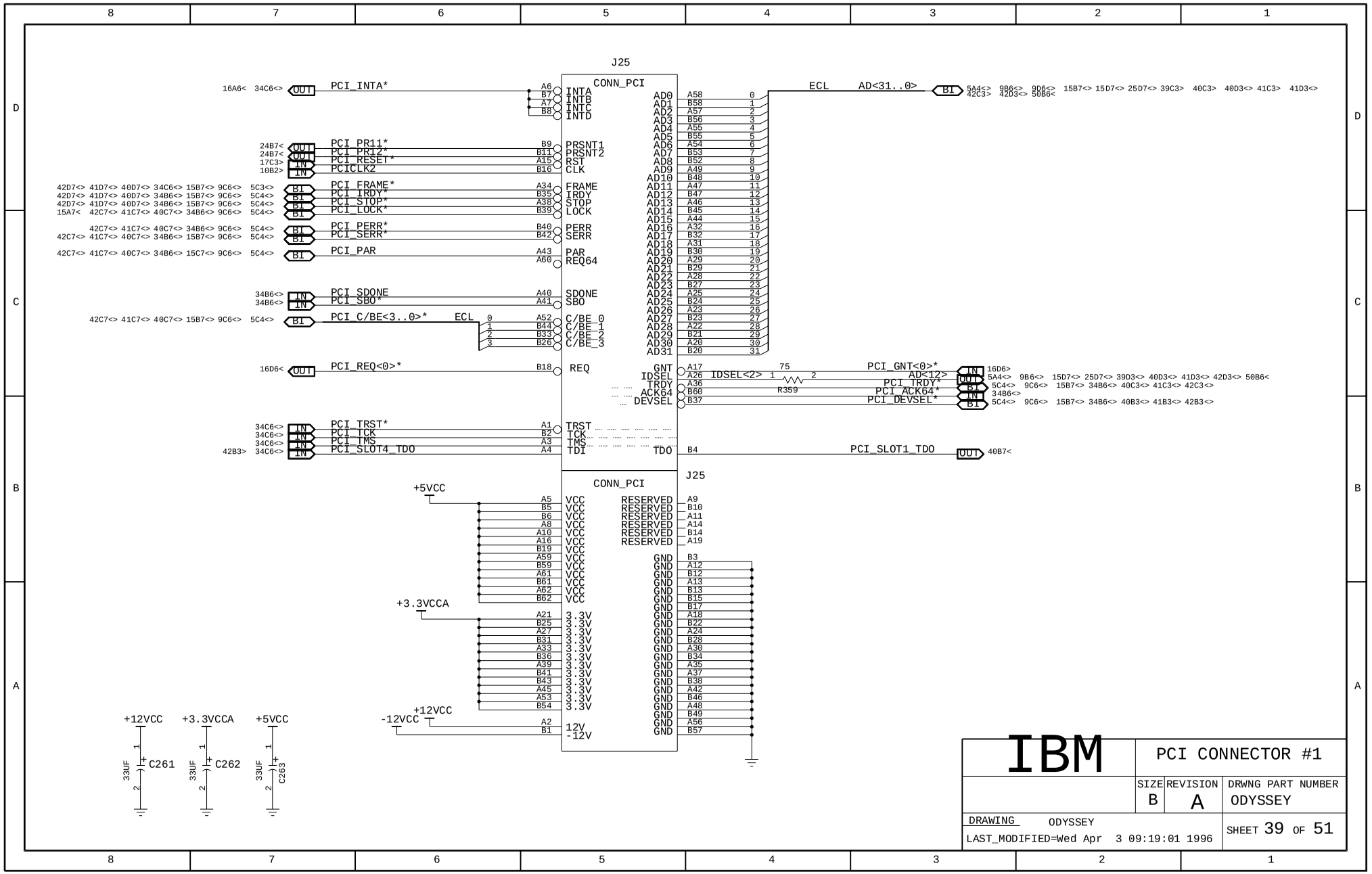


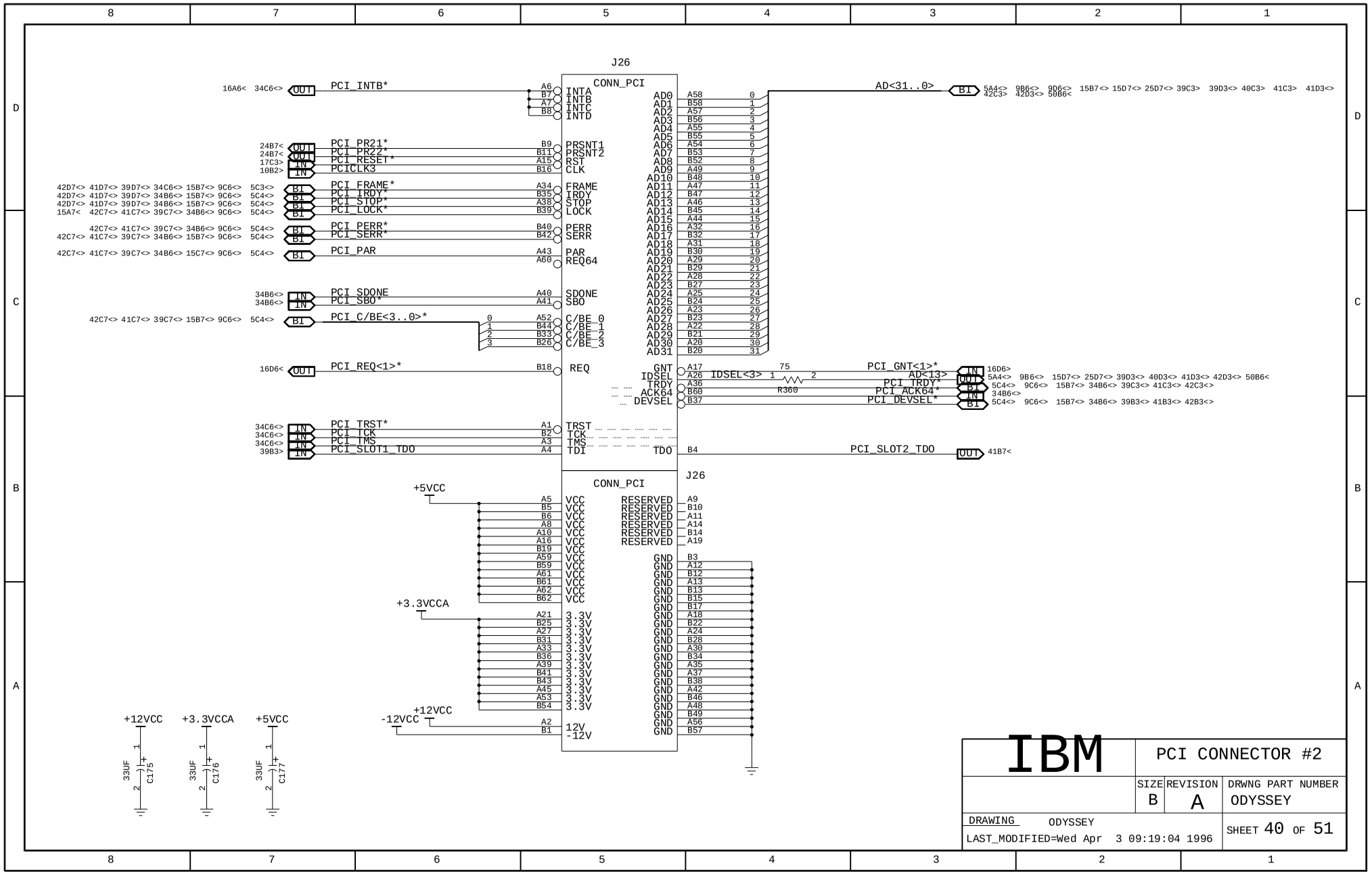
SPARE IC SECTIONS

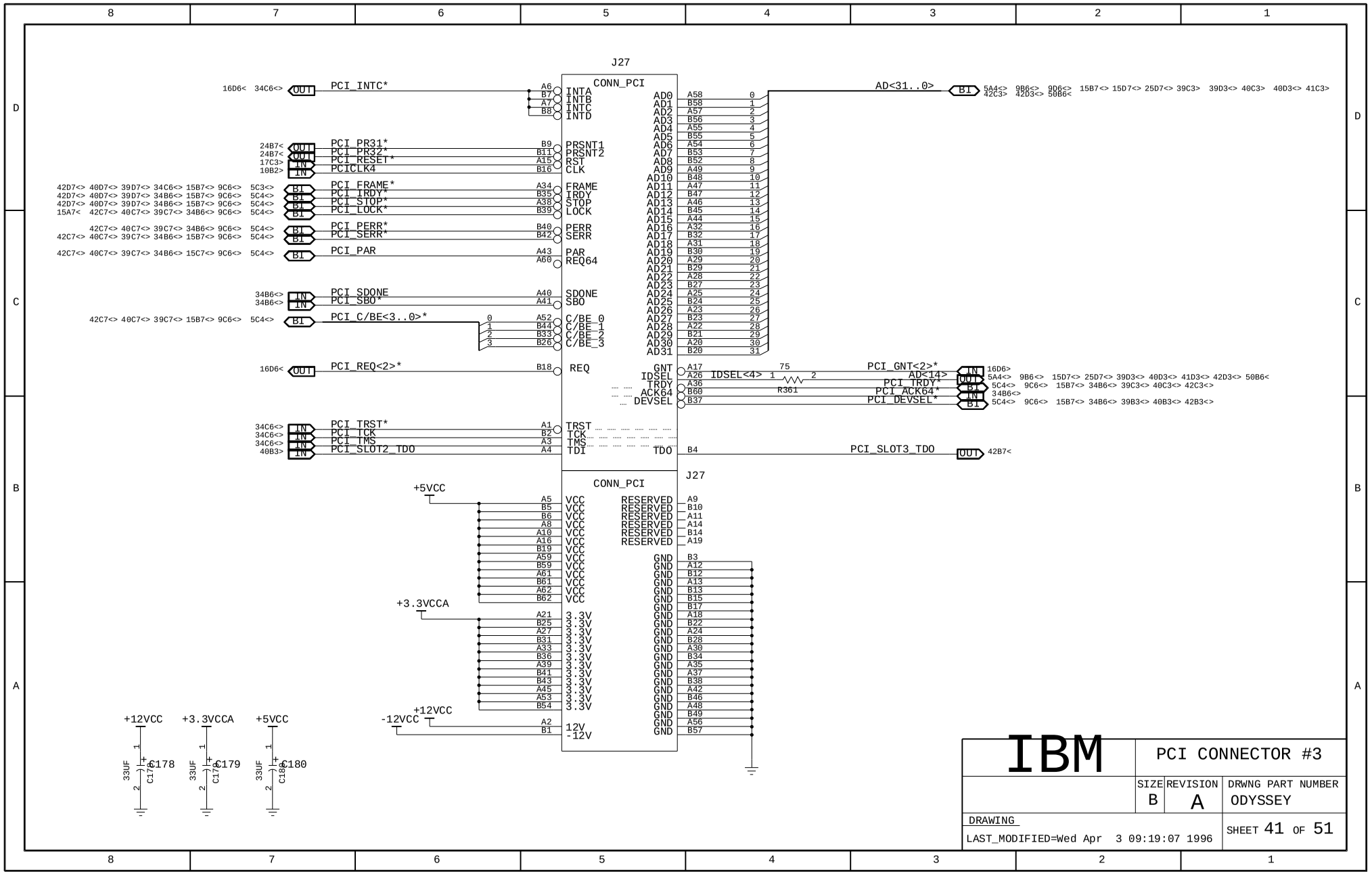
IBM	EMC CAPACITORS & SPARE SECTIONS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:18:50 1996	SHEET 36 OF 51		

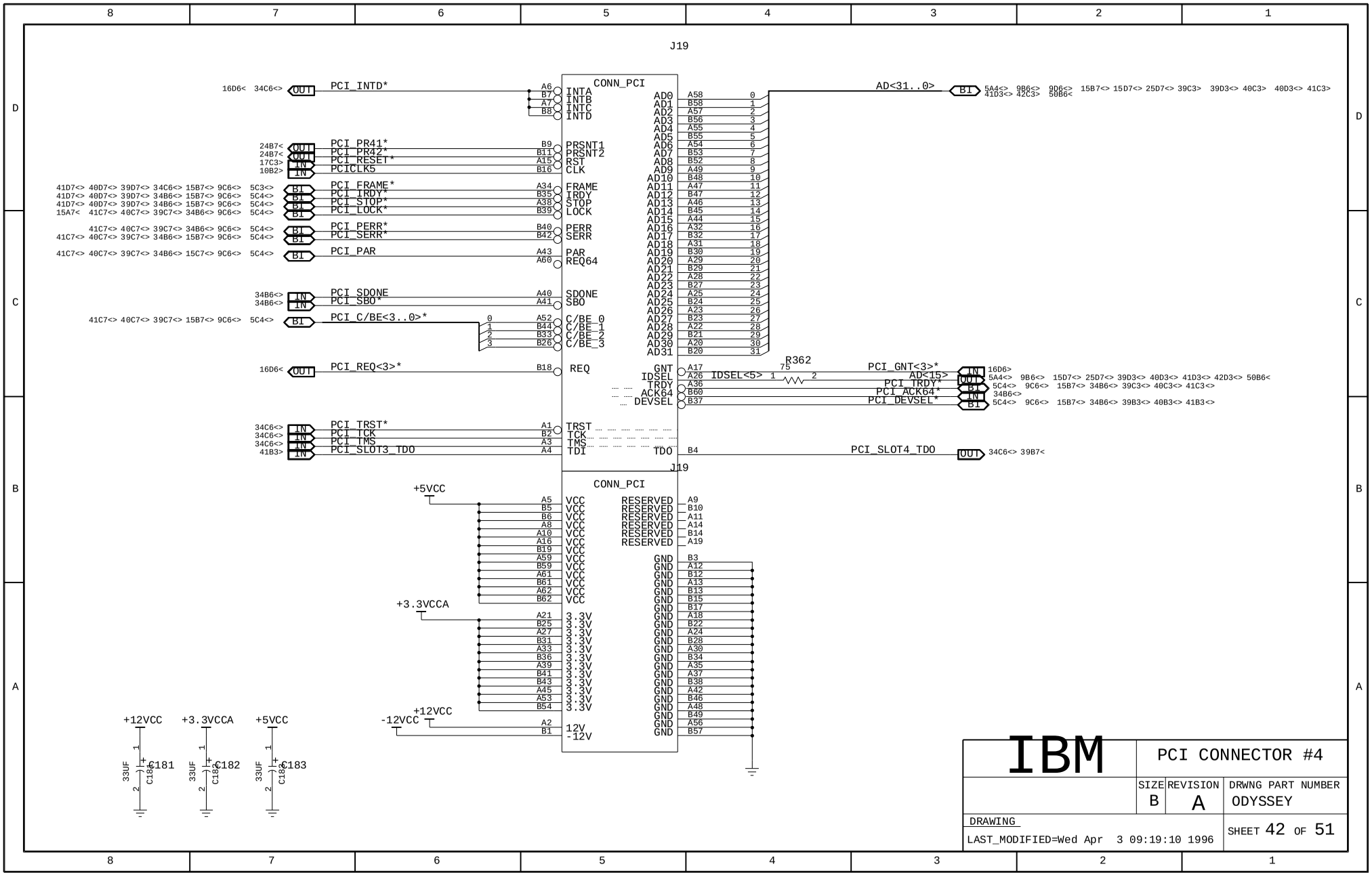

J21
J22
CONN_SIMM72
SIMM 1
SIMM 2
+5VCC
VDD
GND
MRE<1..0>*
MCE<3..0>*
MWE0*
MA<11..0>
MD<31..0>
MDP<3..0>
MPD<7..0>
MCE<7..4>*
MWE1*
MD<63..32>
MDP<7..4>
RAS0
RAS1
RAS2
RAS3
CAS0
CAS1
CAS2
CAS3
CASP
WE
BS3
BS2
BS1
BS0/A11
RESD1
C165
C166
C269
C270
C271
C167
C168
C169
0.01UF
33UF
IBM
MEMORY SIMMS 1 & 2
SIZE B
REVISION A
DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:18:54 1996
SHEET 37 OF 51

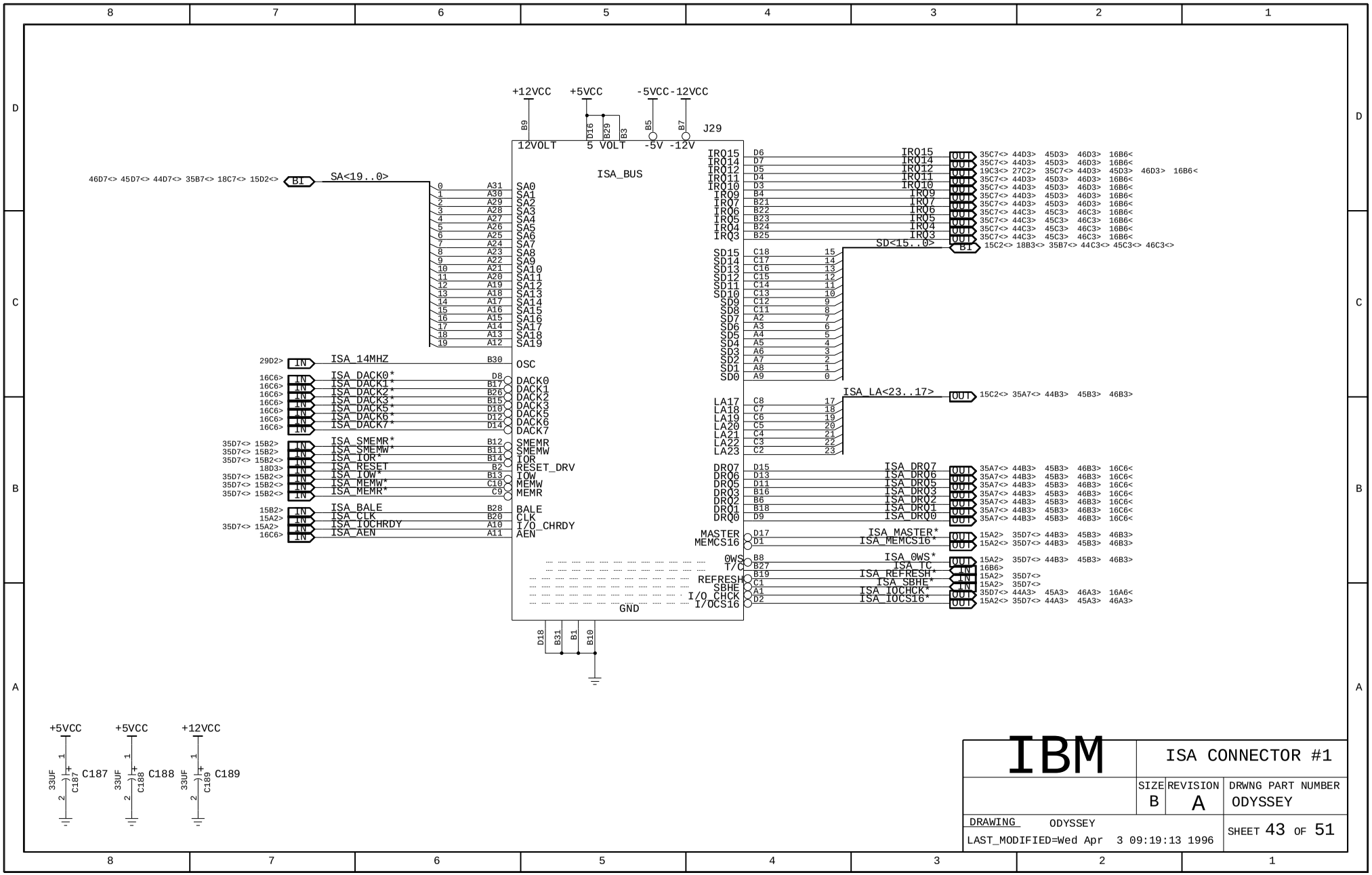

J23
J24
+5VCC
VDD
CONN_SIMM72
SIMM 3
SIMM 4
GND
MRE<3..2>*
MCE<3..0>*
MWE0*
MA<11..0>
MD<31..0>
MDP<3..0>
MPD<15..8>
MCE<7..4>*
MWE1*
MD<63..32>
MDP<7..4>
RAS0
RAS1
RAS2
RAS3
CAS0
CAS1
CAS2
CAS3
CASP
WE
BS3
BS2
BS1
BS0/A11
RESD1
C170
C171
C272
C273
C274
C172
C173
0.01UF
33UF
IBM
MEMORY SIMMS 3 & 4
SIZE B
REVISION A
DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:18:57 1996
SHEET 38 OF 51


J25
CONN_PCI
PCI_INTA*
PCI_PR11*
PCI_PR12*
PCI_RESET*
PCICLK2
PCI_FRAME*
PCI_IRDY*
PCI_STOP*
PCI_LOCK*
PCI_PERR*
PCI_SERR*
PCI_PAR
PCI_SDONE
PCI_SBO*
PCI_C/BE<3..0>*
PCI_REQ<0>*
PCI_TRST*
PCI_TCK
PCI_TMS
PCI_SLOT4_TDO
INTA
INTB
INTC
INTD
PRSNT1
PRSNT2
RST
CLK
FRAME
IRDY
STOP
LOCK
PERR
SERR
PAR
REQ64
SDONE
SBO
C/BE_0
C/BE_1
C/BE_2
C/BE_3
REQ
TRST
TCK
TMS
TDI
TDO
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
ECL AD<31..0>
GNT
IDSEL
TRDY
ACK64
DEVSEL
IDSEL<2>
75
R359
PCI_GNT<0>*
AD<12>
PCI_TRDY*
PCI_ACK64*
PCI_DEVSEL*
PCI_SLOT1_TDO
J25
CONN_PCI
+5VCC
+3.3VCCA
+12VCC
-12VCC
VCC
3.3V
12V
-12V
RESERVED
GND
+12VCC
+3.3VCCA
+5VCC
33UF
C261
C262
C263
IBM
PCI CONNECTOR #1
SIZE
B
REVISION
A
DRWNG PART NUMBER
ODYSSEY
DRAWING
ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:19:01 1996
SHEET 39 OF 51

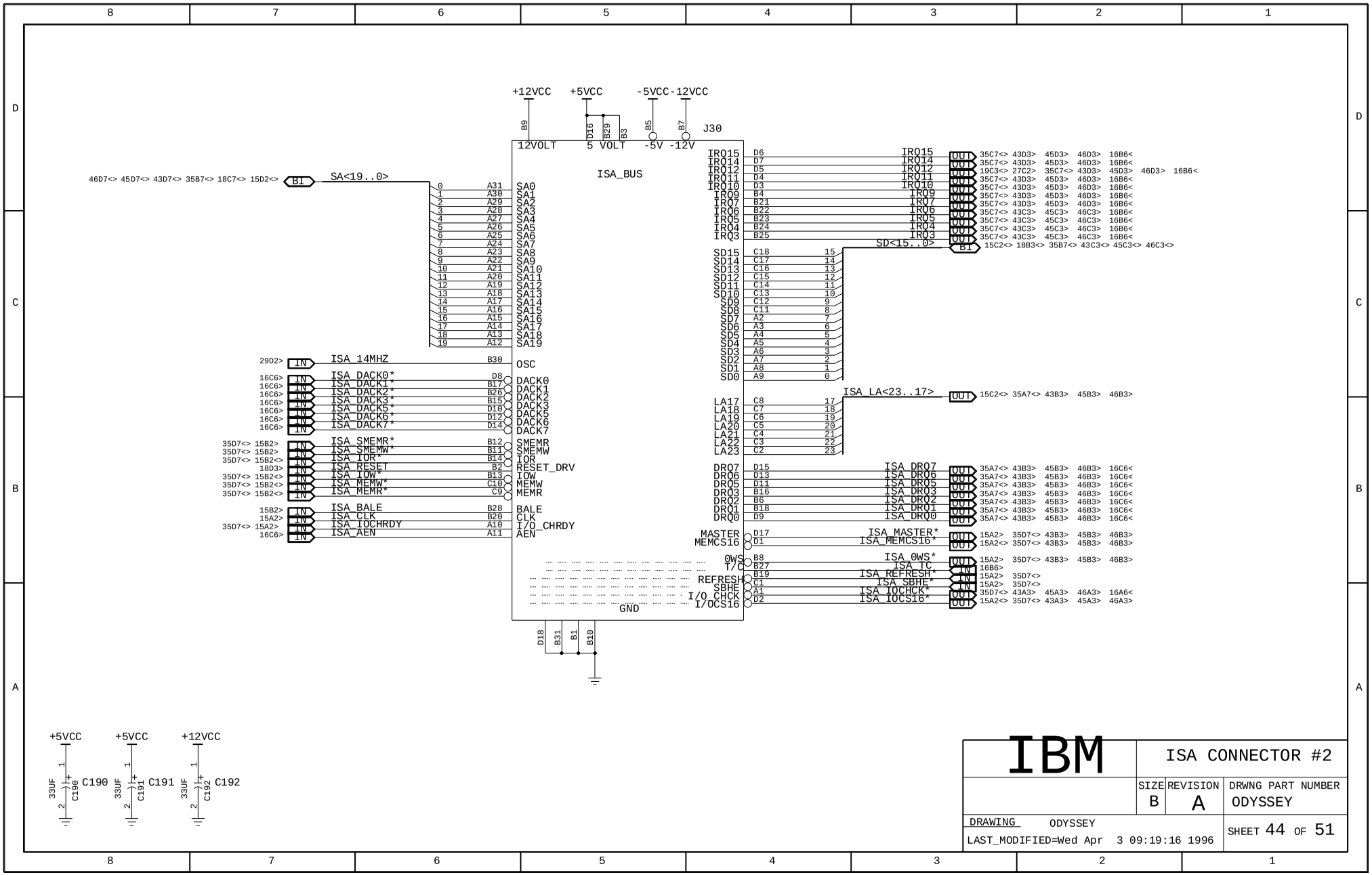

J26
CONN_PCI
PCI_INTB*
INTA
INTB
INTC
INTD
PCI_PR21*
PCI_PR22*
PCI_RESET*
PCICLK3
PRSNT1
PRSNT2
RST
CLK
PCI_FRAME*
PCI_IRDY*
PCI_STOP*
PCI_LOCK*
FRAME
IRDY
STOP
LOCK
PCI_PERR*
PCI_SERR*
PERR
SERR
PCI_PAR
PAR
REQ64
PCI_SDONE
PCI_SBO*
SDONE
SBO
PCI_C/BE<3..0>*
C/BE_0
C/BE_1
C/BE_2
C/BE_3
PCI_REQ<1>*
REQ
PCI_TRST*
PCI_TCK
PCI_TMS
PCI_SLOT1_TDO
TRST
TCK
TMS
TDI
AD<31..0>
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
GNT
IDSEL
TRDY
ACK64
DEVSEL
PCI_GNT<1>*
IDSEL<3>
75
R360
PCI_TRDY*
PCI_ACK64*
PCI_DEVSEL*
TDO
PCI_SLOT2_TDO
J26
CONN_PCI
+5VCC
+3.3VCCA
+12VCC
-12VCC
VCC
3.3V
12V
-12V
RESERVED
GND
+12VCC
+3.3VCCA
+5VCC
33UF
C175
C176
C177
IBM
PCI CONNECTOR #2
SIZE
B
REVISION
A
DRWNG PART NUMBER
ODYSSEY
DRAWING
ODYSSEY
LAST_MODIFIED=Wed Apr 3 09:19:04 1996
SHEET 40 OF 51


J27
CONN_PCI
PCI_INTC*
PCI_PR31*
PCI_PR32*
PCI_RESET*
PCICLK4
PCI_FRAME*
PCI_IRDY*
PCI_STOP*
PCI_LOCK*
PCI_PERR*
PCI_SERR*
PCI_PAR
PCI_SDONE
PCI_SBO*
PCI_C/BE<3..0>*
PCI_REQ<2>*
PCI_TRST*
PCI_TCK
PCI_TMS
PCI_SLOT2_TDO
INTA
INTB
INTC
INTD
PRSNT1
PRSNT2
RST
CLK
FRAME
IRDY
STOP
LOCK
PERR
SERR
PAR
REQ64
SDONE
SBO
C/BE_0
C/BE_1
C/BE_2
C/BE_3
REQ
TRST
TCK
TMS
TDI
AD<31..0>
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
GNT
IDSEL
TRDY
ACK64
DEVSEL
TDO
PCI_GNT<2>*
IDSEL<4>
R361
AD<14>
PCI_TRDY*
PCI_ACK64*
PCI_DEVSEL*
PCI_SLOT3_TDO
J27
CONN_PCI
+5VCC
+3.3VCCA
+12VCC
-12VCC
VCC
3.3V
12V
-12V
RESERVED
GND
+12VCC
+3.3VCCA
+5VCC
33UF
C178
C179
C180
IBM
PCI CONNECTOR #3
SIZE
B
REVISION
A
DRWNG PART NUMBER
ODYSSEY
DRAWING
LAST_MODIFIED=Wed Apr 3 09:19:07 1996
SHEET 41 OF 51

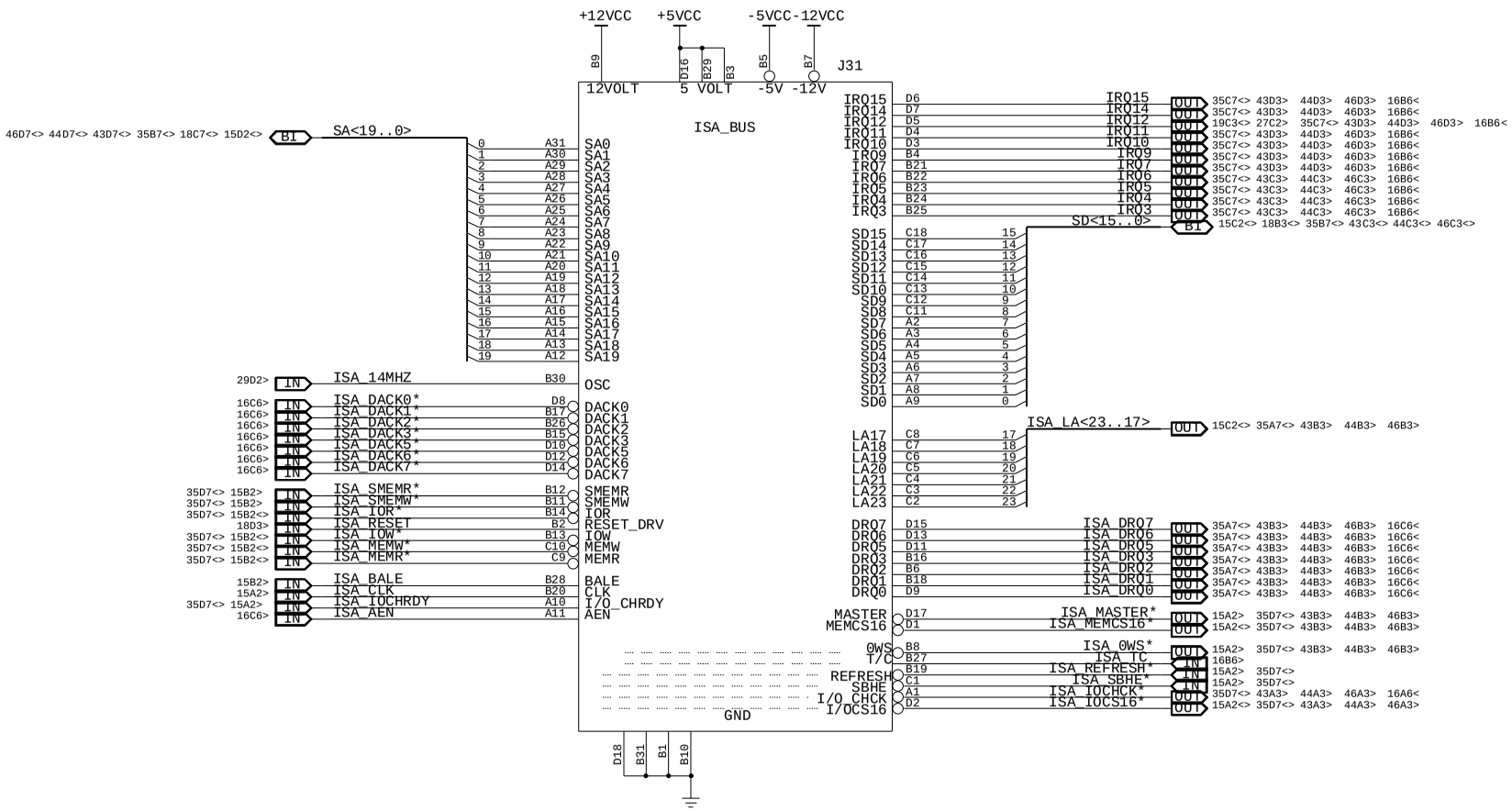

J19
CONN_PCI
PCI_INTD*
PCI_PR41*
PCI_PR42*
PCI_RESET*
PCICLK5
PCI_FRAME*
PCI_IRDY*
PCI_STOP*
PCI_LOCK*
PCI_PERR*
PCI_SERR*
PCI_PAR
PCI_SDONE
PCI_SBO*
PCI_C/BE<3..0>*
PCI_REQ<3>*
PCI_TRST*
PCI_TCK
PCI_TMS
PCI_SLOT3_TDO
AD<31..0>
R362
PCI_GNT<3>*
IDSEL<5>
AD<15>
PCI_TRDY*
PCI_ACK64*
PCI_DEVSEL*
PCI_SLOT4_TDO
J19
CONN_PCI
+5VCC
+3.3VCCA
+12VCC
-12VCC
C181
C182
C183
33UF
IBM
PCI CONNECTOR #4
SIZE B
REVISION A
DRWNG PART NUMBER ODYSSEY
DRAWING
LAST_MODIFIED=Wed Apr 3 09:19:10 1996
SHEET 42 OF 51



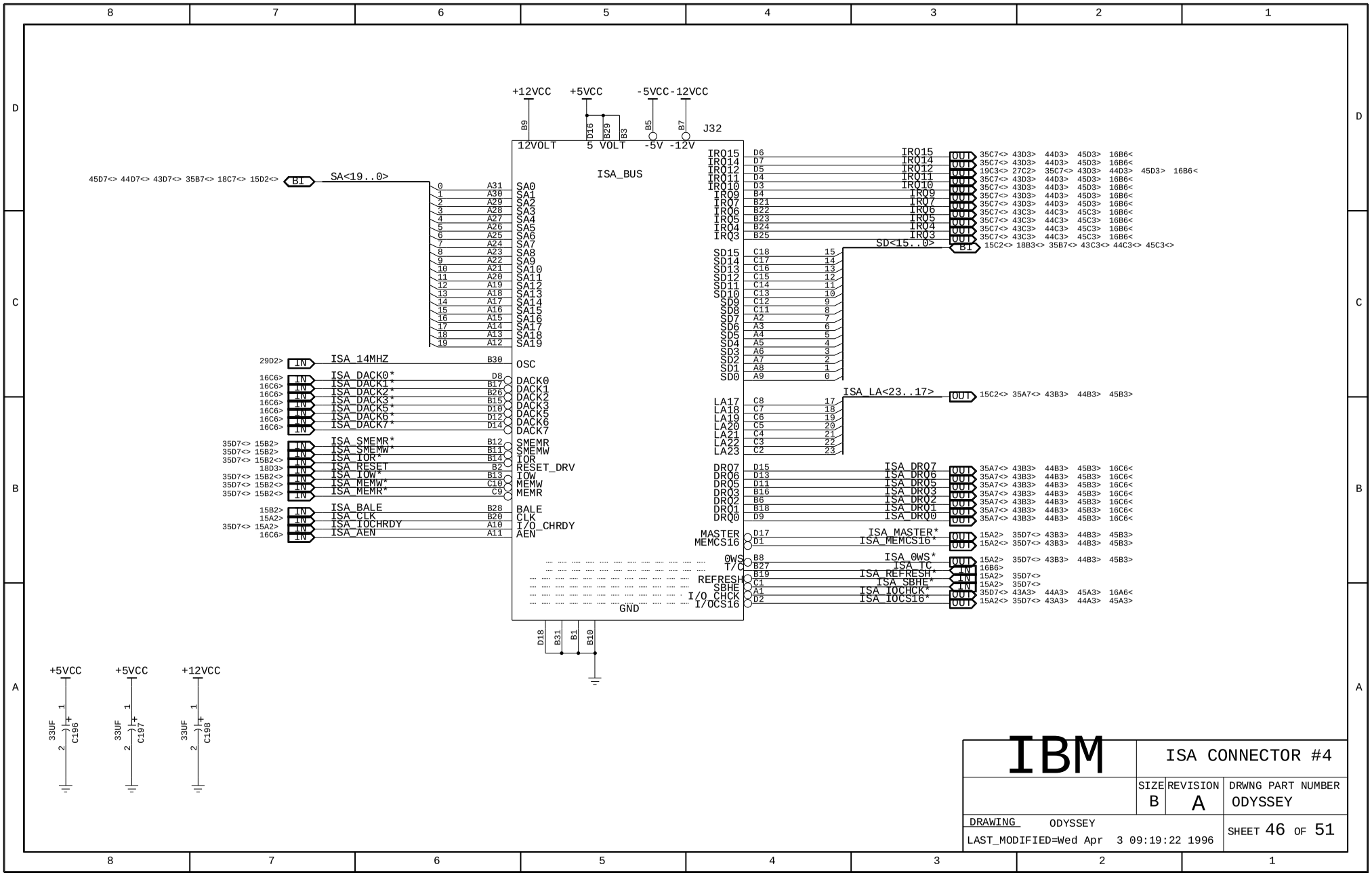
IBM	ISA CONNECTOR #1		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY			SHEET 43 OF 51
LAST_MODIFIED=Wed Apr 3 09:19:13 1996			



IBM	ISA CONNECTOR #2		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY			SHEET 44 OF 51
LAST_MODIFIED=Wed Apr 3 09:19:16 1996			



IBM	ISA CONNECTOR #3		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY			SHEET 45 OF 51
LAST_MODIFIED=Wed Apr 3 09:19:19 1996			



IBM	ISA CONNECTOR #4		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY			SHEET 46 OF 51
LAST_MODIFIED=Wed Apr 3 09:19:22 1996			

BLANK

IBM	BLANK		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Thu Feb 8 15:00:41 1996	SHEET 47 OF 51		

BLANK

IBM

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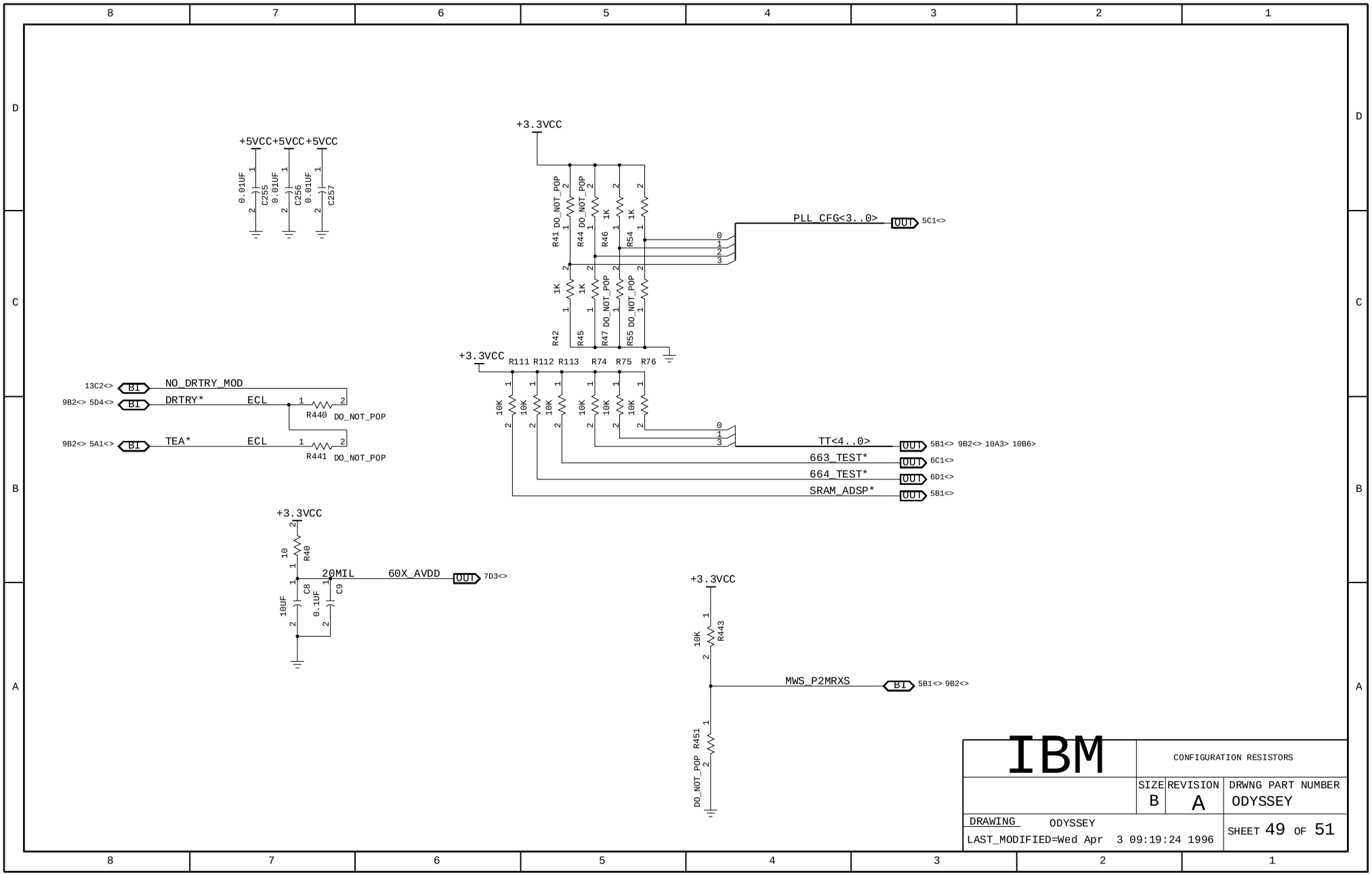
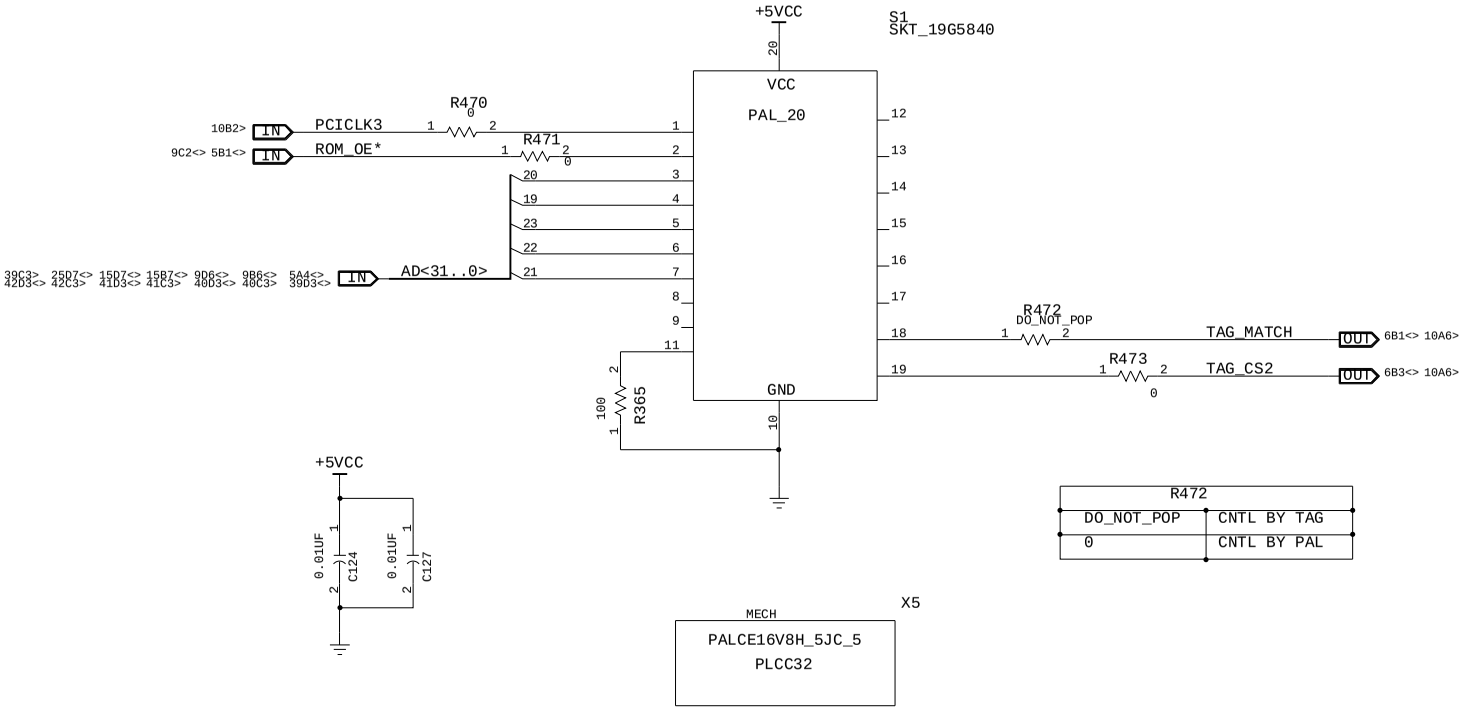
SIZE	REVISION	DRWNG PART NUMBER
B	A	ODYSSEY

DRAWING ODYSSEY

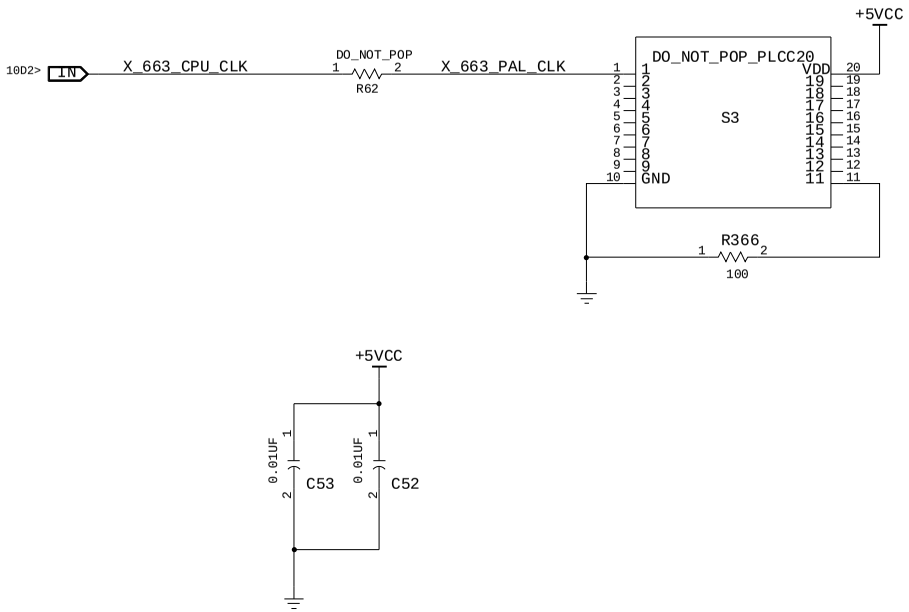
LAST_MODIFIED=Mon Jan 29 16:05:09 1996



IBM	CONFIGURATION RESISTORS		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:19:24 1996	SHEET 49 OF 51		



IBM	TAG_MATCH CONTROL		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:19:27 1996	SHEET 50 OF 51		



IBM	SPARE PAL		
	SIZE B	REVISION A	DRWNG PART NUMBER ODYSSEY
DRAWING ODYSSEY LAST_MODIFIED=Wed Apr 3 09:19:29 1996	SHEET 51 OF 51		

*** Signal Cross-Reference ***
--- for the entire design --

```
60X_AVDD          7D3<> 49B6>
60X_CLK_OUT       6B1<>
603E_CSE0 *       6C3<>
663_CPU_CLK       5C6> 10D5<
663_CPU_PAR_ERR * 6B1<>
663_MEM_ERR *     6B1<>
663_MIO_TEST      5B1<> 9B2<> 10B6>
663_SBE *         6B1<>
663_TEST *        6C1<> 49B3>
664_CPU_CLK       5C1<> 10C5<
664_MIO_TEST      6D1<> 10C6>
664_PCI_CLK       6C3> 10A5<
664_STOP_CLK_EN * 5B1<> 9B2<> 10A6>
664_TEST *        6D1<> 49B3>
A <31..0>         6D5<> 6A4<
AACK *            6C3<>
ABB *             6B3<>
ABUF <28..13>     6B5<>
AD <31..0>        5A4<> 9B6<> 9D6<> 15B7<> 15D7<>
                  25D7<> 39C3> 39D3<> 40C3> 40D3<>
                  41C3> 41D3<> 42C3> 42D3<> 50B6<
AEN_SIO           16C5
AOS_RR_MMRS       6B1<>
AP <3..0>         6C5<>
APE_60X *         6B1<>
ARTRY *           6C3<>
AUX_CN            21C5
AUX_PWR           21C3> 31C2<
AUX_PWR_CNTL      21B3> 31C2<
BALE_SIO *        15B4
BAT_PWR           30A6
BG_60X *          6B3<>
BG_664 *          6B3<>
BG_MASTER *       6B1<> 10A6>
BR_60X *          6B3<>
BR_664 *          6B3<>
BR_MASTER *       5C4<> 9D6<>
BUFF_MAN_RESET    28C4
BUFF_MAN_RESET * 28C2> 28C7<
BUFF_PS_POWER_GOOD 28D2> 28C7<
C2P_WRL_OPEN      6C1<>
CI_60X *          5B1<>
CKSTP_IN *        6C1<>
CKSTP_OUT *       5D4<> 9D6<> 13B7<
CLK_BCLK_DIV0     10D6> 5C6<
CLK_BCLK_DIV1     5C1<> 10D6>
CLK_COM_FRZ       5C1<>
CLK_EXT_FB        5D1<>
CLK_FB_SEL        5D1<>
CLK_FRZ_STROBE    5C1<>
CLK_INV_CLK       9B2<> 10B6>
CLK_MPC601_CLKS   5D1<> 10D6>
CLK_MR/TRISTATE   5D1<> 9A2<> 10B6>
CLK_PCI_DIV0      5C1<> 10D6>
CLK_PCI_DIV1      5C1<> 10D6>
CLK_PLL_EN        5B1<> 9D2<>
CLK_QSYNC         9A2<>
CLK_REF_SEL       5D1<> 9D2<>
CLK_TCLK0         9D2<>
CLK_TCLK1         9D2<>
CLK_TCLK_SEL      9D2<>
CLK_TTL_CLK       5D4<>
CLK_VCO_SEL       5D1<> 9D2<> 10D6>
```

```
CPU_DATA_OE *     6C1<>
CPU_GNT *         9D6<> 15A7>
CPU_GNT_664 *     5C4<> 9D6<>
CPU_RDL_OPEN      6C2
CPU_REQ *         5C4<> 9D6<> 15A7<
CRS_C2PWXS        5B1<> 9C2<> 10B6>
CSE               6C3<>
D <63..0>         6D7<>
DBB *             6C3<>
DBDIS *           6B3<>
DBG_60X *         6D1<> 10B6>
DBWO_60X *        6C1<>
DIR_245_A         6B1<> 10C6>
DIR_245_B         6B1<> 10C6>
DP <7..0>         6C3>
DPE_60X *         6C1<>
DRAM_PD1_RD *     19B3> 22B6<
DRAM_PD2_RD *     19B3> 22A6<
DRTRY *           5D4<> 9B2<> 49B8<>
DUAL_CTRL_REF     6D1<>
ECC_LE_SEL        6D1<>
ECSADDR0          16B3> 19D6<
ECSADDR1          16B3> 19D6<
ECSADDR2          16B3> 19D6<
ECSEN *           16C3> 19D6<
EQP_PD_RD *       19B3> 24A7<
FLUSH_REQ *       15A7> 16D6<
FRZ_CLK           5C1<> 9A2<> 10A2>
FRZ_DATA          5C1<> 9A2<> 10D6> 19A3>
GBL *             6C3<> 10C6>
HDD_LED           28B2> 31A7>
HDD_LED *         19B3> 28B7<
HDWR_RESET *      13B4
HRESET *          5C1<> 9C2<> 13B2>
HRESET_60X        13C3
IDSEL <5..1>      15B6 39C4 40C4 41C4 42C4
IGN_PCI_AD31      5C4<> 9C6<> 18A3>
INT_60X *         5A1<> 6C1<>
INT_TO_664        5B1<> 9B2<> 16A6>
IOR_BUF *         18D5
IOR_SIO *         15B4
IOW_BUF *         18D5
IOW_SIO *         15B4
IRQ1              19B6> 35C7<> 16B6<
IRQ1_IN           27C2> 19C3<
IRQ3              35C7<> 43C3> 44C3> 45C3> 46C3>
                  16B6<
IRQ4              35C7<> 43C3> 44C3> 45C3> 46C3>
                  16B6<
IRQ5              35C7<> 43C3> 44C3> 45C3> 46C3>
                  16B6<
IRQ6              35C7<> 43C3> 44C3> 45C3> 46C3>
                  16B6<
IRQ7              35C7<> 43D3> 44D3> 45D3> 46D3>
                  16B6<
IRQ8 *            26C3> 35C7<> 16B6<
IRQ9              35C7<> 43D3> 44D3> 45D3> 46D3>
                  16B6<
IRQ10             35C7<> 43D3> 44D3> 45D3> 46D3>
                  16B6<
IRQ11             35C7<> 43D3> 44D3> 45D3> 46D3>
                  16B6<
IRQ12             19C3<> 27C2> 35C7<> 43D3> 44D3>
                  45D3> 46D3> 16B6<
IRQ13             16B6
```

```
IRQ14             35C7<> 43D3> 44D3> 45D3> 46D3>
                  16B6<
IRQ15             35C7<> 43D3> 44D3> 45D3> 46D3>
                  16B6<
ISA_0WS *         15A2> 35D7<> 43B3> 44B3> 45B3>
                  46B3>
ISA_14MHZ         29D2> 16B6< 43C7< 44C7< 45C7< 46C7<

ISA_14MHZ_R       29D4
ISA_AEN           16C6> 43B7< 44B7< 45B7< 46B7<
ISA_BALE          15B2> 43B7< 44B7< 45B7< 46B7<
ISA_CLK           15A2> 10A5< 19B6< 43B7< 44B7< 45B7<
                  46B7<
ISA_DACK0 *       16C6> 43C7< 44C7< 45C7< 46C7<
ISA_DACK1 *       16C6> 43C7< 44C7< 45C7< 46C7<
ISA_DACK2 *       16C6> 43B7< 44B7< 45B7< 46B7<
ISA_DACK3 *       16C6> 43B7< 44B7< 45B7< 46B7<
ISA_DACK5 *       16C6> 43B7< 44B7< 45B7< 46B7<
ISA_DACK6 *       16C6> 43B7< 44B7< 45B7< 46B7<
ISA_DACK7 *       16C6> 43B7< 44B7< 45B7< 46B7<
ISA_DRQ0          35A7<> 43B3> 44B3> 45B3> 46B3>
                  16C6<
ISA_DRQ1          35A7<> 43B3> 44B3> 45B3> 46B3>
                  16C6<
ISA_DRQ2          35A7<> 43B3> 44B3> 45B3> 46B3>
                  16C6<
ISA_DRQ3          35A7<> 43B3> 44B3> 45B3> 46B3>
                  16C6<
ISA_DRQ5          35A7<> 43B3> 44B3> 45B3> 46B3>
                  16C6<
ISA_DRQ6          35A7<> 43B3> 44B3> 45B3> 46B3>
                  16C6<
ISA_DRQ7          35A7<> 43B3> 44B3> 45B3> 46B3>
                  16C6<
ISA_IOCHCK *      35D7<> 43A3> 44A3> 45A3> 46A3>
                  16A6<
ISA_IOCHRDY       15A2> 35D7<> 43B7< 44B7< 45B7<
                  46B7<
ISA_IOCS16 *      15A2<> 35D7<> 43A3> 44A3> 45A3>
                  46A3>
ISA_IOR *         15B2<> 35D7<> 18D7< 43B7< 44B7<
                  45B7< 46B7<
ISA_IOW *         15B2<> 35D7<> 18D7< 43B7< 44B7<
                  45B7< 46B7<
ISA_LA <23..17> 15C2<> 35A7<> 43B3> 44B3> 45B3>
                  46B3>
ISA_MASTER *      15A2> 35D7<> 43B3> 44B3> 45B3>
                  46B3>
ISA_MEMCS16 *     15A2<> 35D7<> 43B3> 44B3> 45B3>
                  46B3>
ISA_MEMR *        15B2<> 35D7<> 43B7< 44B7< 45B7<
                  46B7<
ISA_MEMW *        15B2<> 35D7<> 43B7< 44B7< 45B7<
                  46B7<
ISA_REFRESH *     15A2> 35D7<> 43B3< 44B3< 45B3<
                  46B3<
ISA_RESET         18D3> 43B7< 44B7< 45B7< 46B7<
ISA_RESET *       18D3> 27C7<
ISA_SBHE *        15A2> 35D7<> 43B3< 44B3< 45B3<
                  46B3<
ISA_SMEMR *       15B2> 35D7<> 43B7< 44B7< 45B7<
                  46B7<
ISA_SMEMW *       15B2> 35D7<> 43B7< 44B7< 45B7<
                  46B7<
ISA_TC            16B6> 43B3< 44B3< 45B3< 46B3<
KB_CLK_12MHZ      29A3> 27C7<
```

```
KEYLOCK *         31B2> 27D2<
KYBD/MSE_FUSE_GOOD 27A7> 27C2<
KYBD/MSE_GND      27B2> 32B2< 32C2< 32D7<
KYBD/MSE_VCC      27B2> 32D7<> 32B2< 32D2<
KYBD_CLK          27C2<> 27B7<
KYBD_CLK *        27B2<> 27A7< 27D7<
KYBD_CLK_CONN * 27B2<> 32D2<> 32D7<> 27A7<
KYBD_CS *         19B3> 27C7<
KYBD_DATA         27C2<> 27B7<
KYBD_DATA *       27B2<> 27C2<> 27A7<
KYBD_DATA_CONN * 27B2<> 32D2<> 32D7<> 27A7<
KYBD_EA           27A7> 27C7<
KYBD_SS *         27A7> 27C7<
L1_TST_CLK *      6B1<>
L2_CLAIM *        5C4<> 9D6<> 10A6>
L2_PD <2..0>      5D1<> 6B3<> 6C1<> 24D7<
L2_PD_RD *        19B3> 24C7<
L2_TST_CLK *      6B1<>
LED_POWER_GOOD/RESET * 31B3
LSSD_MODE *       6B1<>
MA <11..0>        5B6> 8D3> 37B7< 38B7<
MAN_RESET *       31A7> 28C7<
MAN_RESET_R *     28C5
MCE <7..0> *      5B6> 8C3> 37C2< 37C7< 38C2< 38C7<
MCP_60X *         5D1<> 6C1<>
MD <63..0>        5D7<> 8B3<> 8D5<> 37B2<> 37B8<>
                  38B2<> 38B8<>
MDP <7..0>        5B6> 8B3<> 37A2<> 37A8<> 38A2<>
                  38A8<>
MEMR_SIO *        15B4
MEMW_SIO *        15B4
MEM_BE <3..0>     6D1<>
MEM_DATA_OE *     6C1<>
MEM_RD_SMPL       6C1<>
MEM_WRL_OPEN      6C1<>
MOUSE_CLK         27C2<> 27B7<
MOUSE_CLK *       27B2<> 27A7< 27D7<
MOUSE_CLK_CONN * 27B2<> 32B2<> 27A7<
MOUSE_DATA        27C2<> 27B7<
MOUSE_DATA *      27B2<> 27C2<> 27A7<
MOUSE_DATA_CONN * 27B2<> 32B2<> 27A7<
MPD <15..0>       37D2> 38D2> 22C6<
MRE <7..0> *      5C6> 8A5> 37D7< 38D7<
MWE0 *            5B1<> 9C2<> 37C7< 38C7<
MWE1 *            5B1<> 9C2<> 37C2< 38C2<
MWS_P2MRXS        5B1<> 9B2<> 49A3<>
NMI_FROM_ISABRDG 5B1<> 9B2<> 16A6>
NO_DRTRY_MOD      13C2<> 49C8<>
NVRAM_AS0 *       19B3> 26C6<
NVRAM_AS1 *       19B3> 26C6<
NVRAM_RD *        19B3> 26C6<
NVRAM_WR *        19B3> 26B6<
OE_245_B          6B1<> 10C6>
OSCL_14MHZ_VCC    29D5
OSC_24MHZ         29A6
PCICLK1           10A2> 15C7<
PCICLK2           10B2> 39D7<
PCICLK3           10B2> 40D7< 50C7<
PCICLK4           10B2> 41D7<
PCICLK5           10B2> 42D7<
PCI_ACK64 *       34B6<> 39B3< 40B3< 41B3< 42B3<
PCI_AD_OE *       6C1<>
PCI_C/BE <3..0> * 5C4<> 9C6<> 15B7<> 39C7<> 40C7<>
                  41C7<> 42C7<>
PCI_CLK_IN        10A2> 5D4<
```

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```
PCI_DEVSEL *    5C4<> 9C6<> 15B7<> 34B6<> 39B3<>
                40B3<> 41B3<> 42B3<>
PCI_EXT_SEL     6C1<>
PCI_FRAME *     5C3<> 9C6<> 15B7<> 34C6<> 39D7<>
                40D7<> 41D7<> 42D7<>
PCI_FRAME_664 * 5C5
PCI_GNT <3..0> * 16D6> 18A7< 39C3< 40C3< 41C3<
                42C3<
PCI_INTA *      34C6<> 39D7> 16A6<
PCI_INTB *      34C6<> 40D7> 16A6<
PCI_INTC *      34C6<> 41D7> 16D6<
PCI_INTD *      34C6<> 42D7> 16D6<
PCI_IRDY *      5C4<> 9C6<> 15B7<> 34B6<> 39D7<>
                40D7<> 41D7<> 42D7<>
PCI_LOCK *      5C4<> 9C6<> 34B6<> 39C7<> 40C7<>
                41C7<> 42C7<> 15A7<
PCI_OL_OPEN     6C1<>
PCI_OUT_SEL     6C1<>
PCI_PAR         5C4<> 9C6<> 15C7<> 34B6<> 39C7<>
                40C7<> 41C7<> 42C7<>
PCI_PERR *      5C4<> 9C6<> 34B6<> 39C7<> 40C7<>
                41C7<> 42C7<>
PCI_PR11 *      39D7> 24B7<
PCI_PR12 *      39D7> 24B7<
PCI_PR21 *      40D7> 24B7<
PCI_PR22 *      40D7> 24B7<
PCI_PR31 *      41D7> 24B7<
PCI_PR32 *      41D7> 24B7<
PCI_PR41 *      42D7> 24B7<
PCI_PR42 *      42D7> 24B7<
PCI_REQ <3..0> * 39C7> 40C7> 41C7> 42C7> 16D6<
PCI_RESET *     17C3> 15C7< 39D7< 40D7< 41D7< 42D7<

PCI_SBO *       34B6<> 39C7< 40C7< 41C7< 42C7<
PCI_SDONE       34B6<> 39C7< 40C7< 41C7< 42C7<
PCI_SERR *      5C4<> 9C6<> 15B7<> 34B6<> 39C7<>
                40C7<> 41C7<> 42C7<>
PCI_SLOT1_TDO   39B3> 40B7<
PCI_SLOT2_TDO   40B3> 41B7<
PCI_SLOT3_TDO   41B3> 42B7<
PCI_SLOT4_TDO   34C6<> 42B3> 39B7<
PCI_STOP *      5C4<> 9C6<> 15B7<> 34B6<> 39D7<>
                40D7<> 41D7<> 42D7<>
PCI_TCK         34C6<> 39B7< 40B7< 41B7< 42B7<
PCI_TMS         34C6<> 39B7< 40B7< 41B7< 42B7<
PCI_TRDY *      5C4<> 9C6<> 15B7<> 34B6<> 39C3<>
                40C3<> 41C3<> 42C3<>
PCI_TRST *      34C6<> 39B7< 40B7< 41B7< 42B7<
PCLK_60X        6C3> 10D5<
PLANAR_ID <7..0> 23B4
PLANAR_ID_RD *  19B3> 23B7<
PLL_CFG <3..0>  5C1<> 49C3>
POWER_GOOD/RESET * 28C2> 17C7<
PS_POWER_GOOD   31D7> 28D7<
PS_POWER_GOOD_R * 28D4
QACK_60X *      5B1<> 13C2>
RESETDRV        15A2> 18D7<
RESETDRV_SIO    15A4
RESET_INTERRUPT * 13B4
ROM_LOAD        6B1<>
ROM_OE *        5B1<> 9C2<> 25B7< 50C7<
ROM_WE *        5B1<> 9C2<> 25B7<
RSRV_60X *      6C1<>
RTC_ALE         19B3> 26C6<
RTC_CS *        26C5
RTC_RD *        19B3> 26B6<
```

```
RTC_WR *        19B3> 26C6<
RW_TRST *       13B4
SA <19..0>      15D2<> 18C7<> 35B7<> 43D7<> 44D7<>
                45D7<> 46D7<>
SBHE_SIO *      15A4
SD <15..0>      15C2<> 18B3<> 35B7<> 43C3<> 44C3<>
                45C3<> 46C3<>
SHD *           6B1<> 10A6>
SMI *           5C4<> 9A6<> 10A6>
SPKR            16B6
SPKR_CONN *     16B8> 31A2<
SPKR_CONN_R *   31A3
SRAM_ADS/ADDR0  6B1<>
SRAM_ADSP *     5B1<> 49B3>
SRAM_ALE        6B1<>
SRAM_BCLK0      5C1> 10C5<
SRAM_BCLK1      5D4> 10C5<
SRAM_BCLK2      5D4> 10C5<
SRAM_BCLK3      5D4> 10D5<
SRAM_CNT_EN/ADDR1 6B1<>
SRAM_CS *       6B3<> 10B6>
SRAM_OE *       6B1<> 6B5<>
SRAM_PWR        7D2<> 8C6<> 8D8<>
SRAM_WE *       6B1<>
SRESET_60X *    5C1<> 9B2<> 13B2>
SRESET_SIO *    16C3> 13A2<
SWITCH_GD       31B7> 21B7<
SWITCH_P1       21C3> 31B7>
SYSCLK_SIO      15A4
SYS_RESET *     5B1<> 9C2<> 17C3> 13C2< 19C6<
TA *            6C1<>
TAG_ADDR_13     6A4> 6B3<>
TAG_A_IN        6C3<> 10B6>
TAG_BCLK        6C3> 10D5<
TAG_CLEAR *     6B1<>
TAG_CS1 *       5B1<> 9B2<> 10C6>
TAG_CS2         6B3<> 10A6> 50B2>
TAG_DATA_11     6A4> 6B3<>
TAG_DTY         6B3<>
TAG_MATCH       6B1<> 10A6> 50B2>
TAG_PWRDN *     6B3<> 10A6>
TAG_SFUNC       5B1<> 9B2<> 10C6>
TAG_TA *        6B3<>
TAG_VALID       6B1<>
TAG_VLD         6B3<>
TAG_WE *        6B1<>
TAG_WT          6B3<>
TAG_WT_DTY_IN   6B3<>
TAOE *          5A1<> 10A6>
TA_GATES        6B3<>
TBEN_60X *      6C1<>
TBST *          6C3<>
TC <1..0>       6B3<>
TCK             5C1<> 9C2<> 13B2>
TC_SIO          16B5
TDI             5C1<> 9C2<> 13B2>
TDO             5C1<> 9A2<> 13B7<
TEA *           5A1<> 9B2<> 49B8<>
TEST_SIO        16B3
TLBISYNC *      6C1<>
TMS *           5C1<> 9C2<> 13B2>
TRST *          5C1<> 9A2<> 10A6> 13C2>
TS *            6C3<>
TSIZ <2..0>     6B5<>
TT <4..0>       5B1<> 9B2<> 10A3> 10B6> 49B3>
TT2_664         6C3<> 10A5<
```

```
USER_BCLK0      9A2<>
USER_PCICLK1    6D3> 10A5<
USER_PCICLK1_EM 9C6> 10A5<
USER_PCICLK2    6C3> 10B5<
USER_PCICLK2_EM 9C6> 10B5<
USER_PCICLK3    6D3> 10B5<
USER_PCICLK3_EM 9C6> 10B5<
USER_PCICLK4    5C6> 10B5<
USER_PCICLK5    5C6> 10B5<
USER_PCICLK6    6C3> 10B5<
VBAT            30A5> 21C7< 26C6<
VCCOSC          29A7
WT_60X *        5B1<>
XA <7..0>       18C3<> 19D6< 27C7<
XATS *          6C3<>
XBUF_EN *       18B5
XD <15..0>      18B7<> 22C2> 23C2<> 24D2<> 26C3<>
                27D2<> 35A7<> 19C6<
XDEN *          16C3> 18B7<
XDIR            16C3> 18B7<
XIOR *          18D3> 19C6< 27C7<
XIOW *          18D3> 19C6< 27C7<
XTAL1           29C2> 5C6<
XTAL1_EM        9C2<> 29B2>
XTAL1_RTC       29A2> 26C6<
XTAL2           29C2> 5C6<
XTAL2_EM        9D2<> 29B2>
XTAL2_RTC       29A2> 26C3<
X_663_CPU_CLK   10D2> 5A6< 51C7<
X_663_PAL_CLK   51C6
X_664_CPU_CLK   10C2> 5B6<
X_PCLK_60X      10D2> 5A6<
X_SRAM_BCLK0    10C2> 5C1<
X_SRAM_BCLK1    10C2> 5C1<
X_SRAM_BCLK2    10C2> 5B6<
X_SRAM_BCLK3    10D2> 5B6<
X_TAG_BCLK      10D2> 5B6<
```

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	B		ODYSSEY
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*** Unit Cross-Reference ***
--- for the entire design --

```
B1    BATTERY   30A8
C1    CAPACITOR 10A3
C2    CAPACITOR 10A3
C3    CAPACITOR 13C4 13C5
C4    CAPACITOR 13C4
C5    CAPACITOR 13C4
C6    CAPACITOR 6C1
C7    CAPACITOR 10A3
C8    CAPACITOR 49A7
C9    CAPACITOR 49A7
C10   CAPACITOR 10D3
C11   CAPACITOR 10D3
C12   CAPACITOR 10D3
C13   CAPACITOR 10C3
C14   CAPACITOR 10C3
C15   CAPACITOR 10C3
C16   CAPACITOR 10B3
C17   CAPACITOR 10C3
C18   CAPACITOR 10C3
C19   CAPACITOR 10B3
C20   CAPACITOR 10B3
C21   CAPACITOR 10B3
C27   ELCAP     15A7
C28   CAPACITOR 15A7
C29   CAPACITOR 15A6
C30   CAPACITOR 15A6
C31   CAPACITOR 15A6
C32   CAPACITOR 31D2
C33   CAPACITOR 30B7
C34   CAPACITOR 17C6
C35   CAPACITOR 18C6
C36   CAPACITOR 18B6
C37   CAPACITOR 18A5
C38   ELCAP     19A7
C39   CAPACITOR 19A7
C40   CAPACITOR 19A6 19A7
C43   CAPACITOR 21B6
C46   CAPACITOR 22B5 22C5
C47   CAPACITOR 23B3 23C3
C48   CAPACITOR 24C3
C49   CAPACITOR 24B3
C50   CAPACITOR 25A3 25A4
C52   CAPACITOR 51A6
C53   CAPACITOR 51A6
C57   CAPACITOR 29A7
C58   CAPACITOR 29A8
C61   CAPACITOR 30C7
C70   CAPACITOR 29B6
C71   CAPACITOR 29B6
C80   CAPACITOR 26C5
C81   CAPACITOR 27C6
C82   CAPACITOR 27C4
C83   CAPACITOR 27B4
C84   CAPACITOR 27B3
C85   CAPACITOR 27A3
C86   CAPACITOR 27A5
C87   CAPACITOR 27A6
C88   CAPACITOR 27A5
C89   CAPACITOR 27A5
C90   CAPACITOR 27A5
C91   CAPACITOR 28D4
C92   CAPACITOR 28C5
C93   CAPACITOR 28C4
C94   CAPACITOR 29D6
C95   CAPACITOR 29D5
C98   CAPACITOR 29C6
C99   CAPACITOR 29C6
C110  ELCAP     30B5
C112  ELCAP     31D4
C113  ELCAP     31D4
C114  ELCAP     31D4
C115  ELCAP     31D3
C116  ELCAP     31D3
C117  CAPACITOR 31C4
C118  CAPACITOR 31C4
C119  CAPACITOR 31C4
C120  CAPACITOR 31C3
C121  ELCAP     31B4 31C4
C122  ELCAP     31B4 31C4
C123  CAPACITOR 31A6 31B6
C124  CAPACITOR 50A6
C125  CAPACITOR 31B3
C127  CAPACITOR 50A6
C129  CAPACITOR 36D8
C130  CAPACITOR 36D7 36D8
C131  CAPACITOR 36D7
C132  CAPACITOR 36D7
C133  CAPACITOR 36D7
C134  CAPACITOR 36D7
C135  CAPACITOR 36D6 36D7
C136  CAPACITOR 36D6
C137  CAPACITOR 36D6
C138  CAPACITOR 36D6
C139  CAPACITOR 36D6
C140  CAPACITOR 36D5 36D6
C141  CAPACITOR 36D5
C142  CAPACITOR 36D5
C143  CAPACITOR 36D5
C144  CAPACITOR 36D4 36D5
C145  CAPACITOR 36D4
C146  CAPACITOR 36D4
C147  CAPACITOR 36D4
C148  CAPACITOR 36D4
C149  CAPACITOR 36C8
C150  CAPACITOR 36C7
C151  CAPACITOR 28B4
C152  CAPACITOR 36C6
C153  CAPACITOR 36C6
C154  CAPACITOR 36C6
C156  CAPACITOR 36C5
C157  CAPACITOR 36D3
C158  CAPACITOR 36D2 36D3
C159  CAPACITOR 36D2
C160  CAPACITOR 36D2
C161  CAPACITOR 36D2
C162  CAPACITOR 36D1 36D2
C163  CAPACITOR 36D1
C164  CAPACITOR 36D1
C165  ELCAP     37A7
C166  ELCAP     37A7
C167  CAPACITOR 37A6
C168  CAPACITOR 37A6
C169  CAPACITOR 37A6
C170  ELCAP     38A7
C171  ELCAP     38A7
C172  CAPACITOR 38A6
C173  CAPACITOR 38A6
C174  CAPACITOR 38A6
C175  ELCAP     40A8
C176  ELCAP     40A7
C177  ELCAP     40A7
C178  ELCAP     41A8
C179  ELCAP     41A7
C180  ELCAP     41A7
C181  ELCAP     42A8
C182  ELCAP     42A7
C183  ELCAP     42A7
C187  ELCAP     43A8
C188  ELCAP     43A8
C189  ELCAP     43A7
C190  ELCAP     44A8
C191  ELCAP     44A8
C192  ELCAP     44A7
C193  ELCAP     45A8
C194  ELCAP     45A8
C195  ELCAP     45A7
C196  ELCAP     46A8
C197  ELCAP     46A8
C198  ELCAP     46A7
C202  CAPACITOR 7A6
C203  CAPACITOR 7A6
C204  CAPACITOR 7A6
C205  CAPACITOR 7A5
C206  CAPACITOR 7A5
C207  CAPACITOR 7A5
C208  CAPACITOR 7A5
C209  CAPACITOR 7A5
C210  CAPACITOR 7A4
C211  CAPACITOR 7A4
C212  CAPACITOR 7A4
C213  CAPACITOR 7A4
C214  CAPACITOR 7A3
C215  CAPACITOR 7A3
C216  CAPACITOR 8B3
C217  CAPACITOR 8B3
C218  CAPACITOR 8B2
C219  CAPACITOR 8B2
C220  CAPACITOR 8B2
C221  CAPACITOR 8A3
C222  CAPACITOR 8A3
C223  CAPACITOR 8A2
C224  CAPACITOR 8A2
C225  CAPACITOR 8A2
C226  CAPACITOR 30B7
C255  CAPACITOR 49D7
C256  CAPACITOR 49D7
C257  CAPACITOR 49D7
C259  CAPACITOR 22A5
C261  ELCAP     39A8
C262  ELCAP     39A7
C263  ELCAP     39A7
C269  CAPACITOR 37A8
C270  CAPACITOR 37A8
C271  CAPACITOR 37A8
C272  CAPACITOR 38A8
C273  CAPACITOR 38A8
C274  CAPACITOR 38A7
CR1   10MQ040   21C5
CR2   RLS4148   21B5
CR6   8G4756    28D6
CR7   10MQ040   30A5
F1    POLYSWITCH 27B6
FB1   F_BEAD    29A7
FB4   F_BEAD    27B5
FB5   F_BEAD    27B4
FB6   F_BEAD    29D5
J1    CONN_BERG1X3 6A5
J2    ESP_CONN  13C5
J3    PIN1089   5A4 5D2 5D5 5D7 5D8 6D2 6D4 6D6 6D8
                7D1 7D2 7D3 7D4 7D5 7D6 7D7 7D8 7D8
J4    CONNPOWER 31D5
J5    CONNPOWER2 31C5
J6    POWER1X3  31C4
J7    CONN_BERG1X3 6A5
J8    BERG1X2   31B5
J9    BERG1X2   31B5
J10   BERG1X2   31A5
J11   BERG1X2   31A5
J12   BERG1X5   31B4
J13   BERG1X4   31A4
J14   CONNMDIN6 32D4
J14A  CONNDIN5  32D5
J15   CONNMDIN6 32B4
J16   BERG1X2   5A3
J17   CONN_BERG1X3 7B2
J18   CONN_BERG1X3 7B2
J19   CONN_PCI  42B5 42D5
J21   CONNSIMM72 37D5
J22   CONNSIMM72 37D4
J23   CONNSIMM72 38D5
J24   CONNSIMM72 38D4
J25   CONN_PCI  39B5 39D5
J26   CONN_PCI  40B5 40D5
J27   CONN_PCI  41B5 41D5
J29   CONN_ISA  43D4
J30   CONN_ISA  44D4
J31   CONN_ISA  45D4
J32   CONN_ISA  46D4
J35   BERG1X2   31D2
J36   CONNBERG2X36 8D7
J37   CONNBERG2X36 8D4
J38   CONNBERG2X36 9D7
J39   CONNBERG2X36 9D3
J40   CONN_BERG1X3 24D5
J41   CONN_BERG1X3 24D5
J42   CONN_BERG1X3 24D4
M1    CHANDRA   19D4
M2    PLCC32SKT 25C5
M3    CONN_BATTERY 30A7
M4    REGHSINK  30C5
M5    CONNBATT_KELPIE 30A7
MH1   MTGHOLE   36C7
MH3   MTGHOLE   36C6
MH4   MTGHOLE   36C6
MH5   MTGHOLE   36C6
MH7   MTGHOLE   36C5
MH8   MTGHOLE   36C8
Q1    2N7002    21B4
Q6    IRFZ44    30C6
R1    RESISTOR  13C4
R2    RESISTOR  10B8
R3    RESISTOR  10A8
R4    RESISTOR  10A7
R5    RESISTOR  10A8
R6    RESISTOR  10A8
R7    RESISTOR  10A8
R8    RESISTOR  10A8
R9    RESISTOR  30B6
R10   RESISTOR  10A8
R11   RESISTOR  10A8
R12   RESISTOR  10A8
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R13	RESISTOR	10A8
R14	RESISTOR	10D7
R15	RESISTOR	10D7
R16	RESISTOR	10D7
R17	RESISTOR	10D7
R18	RESISTOR	10D7
R19	RESISTOR	10D7
R20	RESISTOR	10D7
R21	RESISTOR	10C7
R22	RESISTOR	10D4
R23	RESISTOR	10D4
R24	RESISTOR	10D4
R25	RESISTOR	10D4
R26	RESISTOR	10C4
R27	RESISTOR	10C4
R28	RESISTOR	10C7
R29	RESISTOR	10C7
R30	RESISTOR	10C4
R31	RESISTOR	10C7
R32	RESISTOR	10C7
R33	RESISTOR	10C7
R34	RESISTOR	10C7
R35	RESISTOR	10C7
R36	RESISTOR	10B7
R37	RESISTOR	10B7
R38	RESISTOR	10B7
R39	RESISTOR	10B7
R40	RESISTOR	49B7
R41	RESISTOR	49C5
R42	RESISTOR	49C5
R43	RESISTOR	6A5
R44	RESISTOR	49C5
R45	RESISTOR	49C5
R46	RESISTOR	49C5
R47	RESISTOR	49C5
R54	RESISTOR	49C5
R55	RESISTOR	49C5
R56	RESISTOR	10A5
R57	RESISTOR	10A5
R58	RESISTOR	10A4
R62	RESISTOR	51C6
R65	RESISTOR	10C4
R66	RESISTOR	10B4
R67	RESISTOR	10B4
R68	RESISTOR	10B4
R69	RESISTOR	10B4
R70	RESISTOR	10B4
R71	RESISTOR	10A4
R72	RESISTOR	10A4
R73	RESISTOR	6C2
R74	RESISTOR	49C5
R75	RESISTOR	49C5
R76	RESISTOR	49C5
R77	RESISTOR	10B7
R78	RESISTOR	10A5
R79	RESISTOR	15B6
R80	RESISTOR	16C6
R81	RESISTOR	15A6
R82	RESISTOR	15B3
R83	RESISTOR	15B3
R84	RESISTOR	15B3
R85	RESISTOR	15B3
R86	RESISTOR	15B3
R87	RESISTOR	15A3
R88	RESISTOR	15A3
R89	RESISTOR	15A3

R90	RESISTOR	16D6
R91	RESISTOR	16D6
R92	RESISTOR	16D6
R93	RESISTOR	16D6
R94	RESISTOR	16A6
R95	RESISTOR	16D5
R96	RESISTOR	16C6
R97	RESISTOR	16C6
R98	RESISTOR	16A6
R99	RESISTOR	16A5
R100	RESISTOR	16B3
R101	RESISTOR	24C5
R102	RESISTOR	15A6
R103	RESISTOR	17C4
R104	RESISTOR	18D4
R105	RESISTOR	18D4
R106	RESISTOR	18B4
R107	RESISTOR	24C4
R108	RESISTOR	24C4
R111	RESISTOR	49C6
R112	RESISTOR	49C5
R113	RESISTOR	49C5
R118	RESISTOR	21B6
R119	RESISTOR	21B5
R120	RESISTOR	21B5
R121	RESISTOR	21B4
R122	RESISTOR	21B4
R123	RESISTOR	21B4
R124	RESISTOR	21B6
R129	RESISTOR	16A5
R130	RESISTOR	16A5
R135	RESISTOR	16D5
R138	RESISTOR	22C6
R139	RESISTOR	22C5
R140	RESISTOR	22C5
R141	RESISTOR	22C5
R142	RESISTOR	22C5
R143	RESISTOR	22C5
R144	RESISTOR	22C4
R145	RESISTOR	22C4
R146	RESISTOR	23C5
R147	RESISTOR	23C5
R148	RESISTOR	23C5
R149	RESISTOR	23C5
R150	RESISTOR	23C4
R151	RESISTOR	23B5
R152	RESISTOR	23B5
R153	RESISTOR	23B5
R154	RESISTOR	23B4
R155	RESISTOR	24C6
R156	RESISTOR	24C6
R157	RESISTOR	24C6
R158	RESISTOR	24C5
R159	RESISTOR	24C5
R160	RESISTOR	24C5
R161	RESISTOR	24C5
R162	RESISTOR	24C5
R163	RESISTOR	24D5
R164	RESISTOR	24D5
R165	RESISTOR	24D4
R166	RESISTOR	24D4
R170	RESISTOR	6A3
R171	RESISTOR	6A3
R172	RESISTOR	5C4
R173	RESISTOR	9D6
R174	RESISTOR	13B4

R176	RESISTOR	25B5
R177	RESISTOR	29A5
R178	RESISTOR	29A6
R189	RESISTOR	23C6
R190	RESISTOR	23B6
R191	RESISTOR	23C6
R192	RESISTOR	23B6
R193	RESISTOR	23C5
R194	RESISTOR	23B5
R225	RESISTOR	26B5
R226	RESISTOR	27B5
R227	RESISTOR	27B5
R228	RESISTOR	27B4
R229	RESISTOR	27B4
R230	RESISTOR	27A5
R231	RESISTOR	27A6
R232	RESISTOR	27A5
R233	RESISTOR	27A5
R234	RESISTOR	27A5
R235	RESISTOR	27A5
R236	RESISTOR	27A4
R237	RESISTOR	28D5
R238	RESISTOR	28D5
R239	RESISTOR	28D6
R240	RESISTOR	28C6
R241	RESISTOR	31B2
R243	RESISTOR	29D3
R245	RESISTOR	29C5
R250	RESISTOR	31A3
R251	RESISTOR	31A2
R253	RESISTOR	34D5
R254	RESISTOR	34D5
R255	RESISTOR	34D5
R256	RESISTOR	34D5
R257	RESISTOR	34D5
R258	RESISTOR	34D4
R259	RESISTOR	34D4
R260	RESISTOR	34D4
R261	RESISTOR	34D4
R262	RESISTOR	34D4
R263	RESISTOR	34D3
R264	RESISTOR	34D3
R265	RESISTOR	34D3
R266	RESISTOR	34D3
R267	RESISTOR	34D3
R268	RESISTOR	34D2
R269	RESISTOR	34D2
R270	RESISTOR	34D2
R271	RESISTOR	34D2
R272	RESISTOR	34D2
R273	RESISTOR	35D6
R274	RESISTOR	35D6
R275	RESISTOR	35D6
R276	RESISTOR	35D5
R277	RESISTOR	35D5
R278	RESISTOR	35D5
R279	RESISTOR	35D5
R280	RESISTOR	35D5
R281	RESISTOR	35D4
R282	RESISTOR	35D4
R283	RESISTOR	35D4
R284	RESISTOR	35D4
R285	RESISTOR	35D4
R286	RESISTOR	35D3
R287	RESISTOR	35D3
R288	RESISTOR	35D3

R289	RESISTOR	35D3
R290	RESISTOR	35D3
R291	RESISTOR	35D2
R292	RESISTOR	35D2
R293	RESISTOR	35D2
R294	RESISTOR	35D2
R295	RESISTOR	35D2
R296	RESISTOR	35D1
R297	RESISTOR	35D1
R298	RESISTOR	16A6
R299	RESISTOR	35D1
R300	RESISTOR	35D1
R301	RESISTOR	35C6
R302	RESISTOR	35C6
R303	RESISTOR	35C6
R304	RESISTOR	35C5
R305	RESISTOR	35C5
R306	RESISTOR	35C5
R307	RESISTOR	35C5
R308	RESISTOR	35C5
R309	RESISTOR	35C4
R310	RESISTOR	35C4
R311	RESISTOR	35C4
R312	RESISTOR	35C4
R313	RESISTOR	35C4
R314	RESISTOR	35C3
R315	RESISTOR	35C3
R316	RESISTOR	35C3
R317	RESISTOR	35C3
R318	RESISTOR	35C3
R319	RESISTOR	35C2
R320	RESISTOR	35C2
R321	RESISTOR	35B6
R322	RESISTOR	35B6
R323	RESISTOR	35B6
R324	RESISTOR	35B5
R325	RESISTOR	35B5
R326	RESISTOR	35B5
R327	RESISTOR	35B5
R328	RESISTOR	35B5
R329	RESISTOR	35B4
R330	RESISTOR	35B4
R331	RESISTOR	35B4
R332	RESISTOR	35B4
R333	RESISTOR	35B4
R334	RESISTOR	35B3
R335	RESISTOR	35B3
R336	RESISTOR	35B3
R337	RESISTOR	35B6
R338	RESISTOR	35B6
R339	RESISTOR	35B6
R340	RESISTOR	35B5
R341	RESISTOR	35B5
R342	RESISTOR	35B5
R343	RESISTOR	35B5
R344	RESISTOR	35B5
R345	RESISTOR	35B4
R346	RESISTOR	35B4
R347	RESISTOR	35B4
R348	RESISTOR	35B4
R349	RESISTOR	35B4
R350	RESISTOR	35B3
R351	RESISTOR	35B3
R352	RESISTOR	35A6
R353	RESISTOR	35A6
R354	RESISTOR	35A6

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R355  RESISTOR  35A5
R356  RESISTOR  35A5
R357  RESISTOR  35A5
R358  RESISTOR  35A5
R359  RESISTOR  39C4
R360  RESISTOR  40C4
R361  RESISTOR  41C4
R362  RESISTOR  42C4
R364  RESISTOR  19B6
R365  RESISTOR  50B5
R366  RESISTOR  51B4
R369  RESISTOR  10B4
R370  RESISTOR  10A4
R372  RESISTOR  10A4
R436  RESISTOR  30C7
R437  RESISTOR  30B6
R440  RESISTOR  49B7
R441  RESISTOR  49B7
R443  RESISTOR  49A4
R451  RESISTOR  49A4
R470  RESISTOR  50C6
R471  RESISTOR  50C6
R472  RESISTOR  50B4
R473  RESISTOR  50B3
R485  RESISTOR  23B5
R488  RESISTOR  22C4
R489  RESISTOR  22C4
R490  RESISTOR  22C4
R491  RESISTOR  22C3
R492  RESISTOR  22C3
R493  RESISTOR  22C3
R494  RESISTOR  22C3
R495  RESISTOR  22C3
R497  RESISTOR  13C3
R505  RESISTOR  31A6
R510  RESISTOR  13B3
R511  RESISTOR  10A4
R512  RESISTOR  10A3
R513  RESISTOR  10B7
S1    PAL_20    50C4
S3    DO-NOT-POP_PLCC20 51C4
U1    F08       13B3 13B3 13C3 36B2
U2    HCT14     18D4 18D5 28C3 28C5 28D3 28D4
U3    06        13C3
U4    LT1431REG 30B6
U5    DS1385    26C4
U7    S82378ZB  15D4 16D4 17B5
U10   F244      17D5 18D5
U11   F244      18C5 18D5
U12   F245      18B5
U13   F11       18A4 18A5 36B2
U16   F125      28B5 36C2
U17   F244      22C4
U18   F244      23B4 23C4
U19   F244      24D3
U20   F244      24B3 24C3
U21   F74       29A5
U27   8042H     27D4
U28   06        16A6 16B8 27B5 27B6
U29   F08       28C5 36C2
U40   F244      22A4 22B4
X1    PART      7A3
X2    EPM5130FP 19A4
X3    29F040ROM_MECH 25A4
X4    PART      7A3
X5    PAL_MECH  50A4
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```
Y1    OSCLR     29D4
Y2    CRYSTL    29C4
Y2A   XTAL      29C5
Y3    CRYSTAL_2PIN 29B4
Y3A   XTAL      29B5
Y4    CRYSTL    29B4
Y4A   XTAL      29B5
Y5    OSCLR     29A6
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Appendix G
Data Sheets

This section contains data sheets on selected components. IBM does not recommend the use of components from any particular manufacturer (other than IBM). The following data sheets are included as reference material only. Third party material is reproduced and included by permission of the copyright owner.

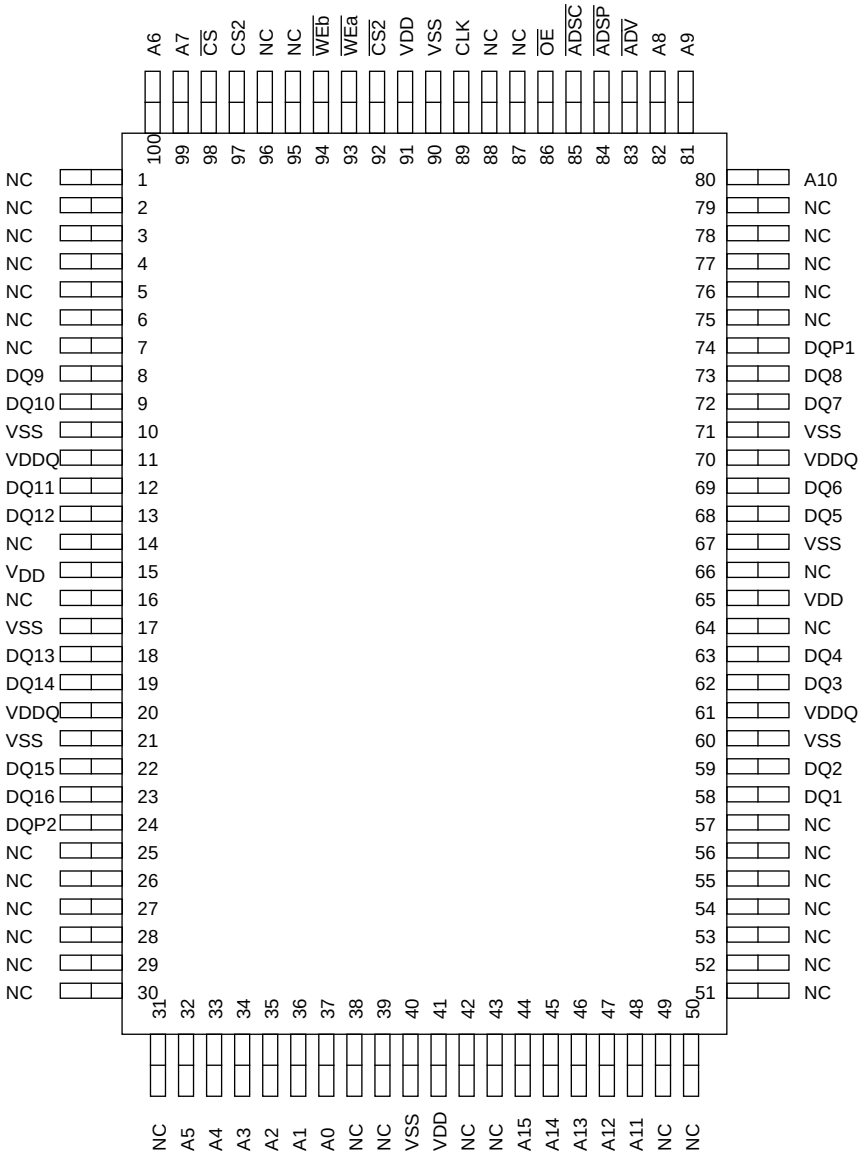
Features

- 64K x 18 Synchronous Burst Mode SRAM
- 0.5µ CMOS Technology
- Synchronous Burst Mode of Operation Compatible with PowerPC™ Processors
- LVTTL I/O Compatible with Common I/O
- Single +3.3 V ± 5% Power Supply and Ground
- Registered Addresses, Data Ins and Control Signals
- 5 V Tolerant I/O
- Asynchronous Output Enable
- Self-Timed Write Operation and Byte Write Capability
- Low Power Dissipation
  - 1.1 W Active at 83MHz
  - 90 mW Standby
- 100 Pin Thin Quad Flat Pack

Description

IBM Microelectronics 1M SRAM is a Synchronous Burstable, high performance CMOS Static RAM that is versatile, wide I/O, and achieves 8 nsec access. A single clock is used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the Clock, all Addresses, Data Ins and Control Signals are registered internally. Burst mode operation, compatible with PowerPC™ Processor's sequence, is accomplished by integrating input registers, internal 2-bit burst counter and high speed SRAM in a single chip. Burst reads are initiated with either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ being LOW with a valid address during the rising edge of clock. Data from this address plus the three subsequent addresses will be output. The chip is operated with a single +3.3 V power supply and is compatible with LVTTL I/O interfaces.

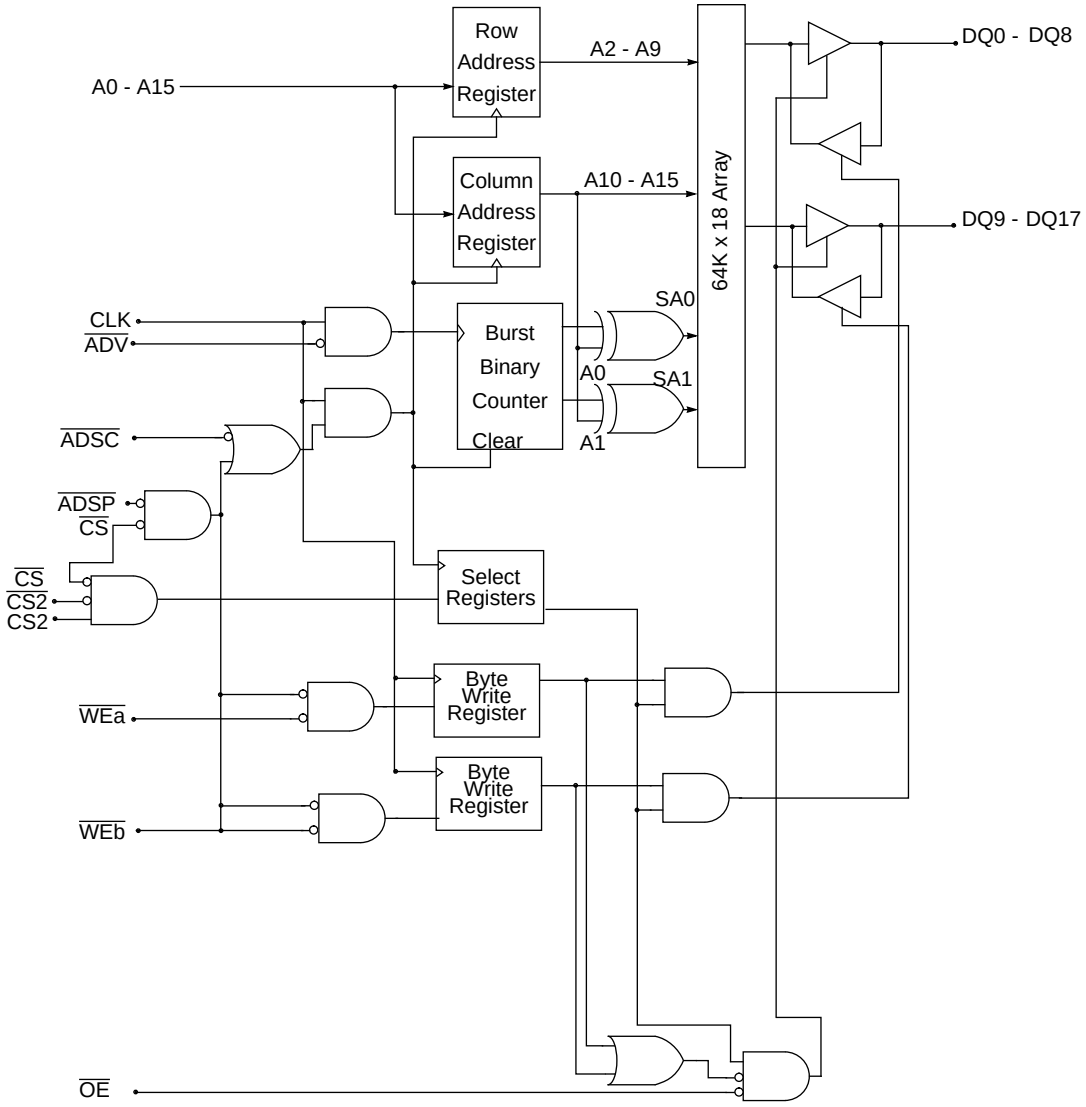
X18 TQFP Pin Array Layout



Pin Description

A0-A15	Address input	$\overline{ADSP}$	Address Status Processor
DQa - DQb	Data Input/Output (1-8 , 9-16)	$\overline{ADSC}$	Address status controller
CLK	Clock	$\overline{ADV}$	Burst Advance Control
$\overline{WEa}$	Write Enable, Byte a (1 to 8 & DQP1)	$\overline{CS}$	$\overline{ADSP}$ - Gated Chip Select
$\overline{WEb}$	Write Enable, Byte b (9 to 16 & DQP2)	V_{DD}	Power Supply (+3.3V)
$\overline{OE}$	Output Enable	V_{SS}	Ground
$\overline{CS2}$, CS2	Chip Selects	V_{DDQ}	Output Power Supply (+3.3V)
DQP1,DQP2	Parity bits for byte a, and byte b.	NC	No Connect

Block Diagram



Ordering Information

Part Number	Organization	Speed	Leads	Notes
IBM041814PQK-8	64K x 18	8 ns Access / 12 ns Cycle	100 pin TQFP	
IBM041814PQK-9	64K x 18	9 ns Access / 12 ns Cycle	100 pin TQFP	
IBM041814PQK-10	64K x 18	10 ns Access / 12 ns Cycle	100 pin TQFP	
IBM041814PQK-11	64K x 18	11 ns Access / 12 ns Cycle	100 pin TQFP	

Burst SRAM Clock Truth Table

CLK	$\overline{CS2}$	CS2	$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	DQ	Operation
L→H	H	X	L	L	X	X	X	X	High-Z	Deselected Cycle
L→H	X	L	L	L	X	X	X	X	High-Z	Deselected Cycle
L→H	H	X	X	X	L	X	X	X	High-Z	Deselected Cycle
L→H	X	L	X	X	L	X	X	X	High-Z	Deselected Cycle
L→H	L	H	L	L	X	X	X	L	Q	Read from External Address, Begin Burst
L→H	L	H	L	L	X	X	X	H	High-Z	Read from External Address, Begin Burst
L→H	L	H	L	H	L	X	H	L	Q	Read from External Address, Begin Burst
L→H	L	H	L	H	L	X	L	X	D	Write to External Address, Begin Burst
L→H	X	X	X	H	H	L	H	L	Q	Read from next Add., Continue Burst
L→H	X	X	X	H	H	L	L	X	D	Write to next Add., Continue Burst
L→H	X	X	X	H	H	H	H	L	Q	Read from Current Add., Suspend Burst
L→H	X	X	X	H	H	H	L	X	D	Write to Current Add., Suspend Burst
L→H	X	X	H	X	L	X	X	X	High-Z	Deselect Cycle
L→H	X	X	H	X	H	L	H	L	Q	Read from next Add., Continue Burst
L→H	X	X	H	X	H	L	L	X	D	Write to next Add., Continue Burst
L→H	X	X	H	X	H	H	H	L	Q	Read from current Add., Suspend Burst
L→H	X	X	H	X	H	H	L	X	D	Write to current Add., Suspend Burst

1. For a write operation preceded by a read cycle, $\overline{OE}$ must be HIGH early enough to allow Input Data Setup, and must be kept HIGH through Input Data Hold Time.
2. $\overline{WE}$ refers to $\overline{WEa}$, $\overline{WEb}$.
3. $\overline{ADSP}$ is gated by $\overline{CS}$, and $\overline{CS}$ is used to block $\overline{ADSP}$ when $\overline{CS}$ = V_{IH}, as required in applications using Processor Address Pipelining.
4. All Addresses, Data In and Control signals are registered on the rising edge of CLK.

Burst Sequence Truth Table

External Address	A15-A2	(A1,A0)				Notes
		(0,0)	(0,1)	(1,0)	(1,1)	
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)	
2nd Access	A15-A2	(0,1)	(1,0)	(1,1)	(0,0)	
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)	
4th Access	A15-A2	(1,1)	(0,0)	(0,1)	(1,0)	

Write Enable Truth Table

$\overline{WEa}$	$\overline{WEb}$	Byte Written	Notes
H	H	Read All Bytes	
L	L	Write All Bytes	
L	H	Write Byte A (D_{IN} 0 - 8)	
H	L	Write Byte B (D_{IN} 9 - 17)	

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.6	V	1
Input Voltage	V_{IN}	-0.5 to 6.0	V	1
Output Voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V	1
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Power Dissipation	P_D	2.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.465	V	1, 4
Input High Voltage	V_{IH}	2.2	—	5.5	V	1, 2, 4
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3, 4
Output Current	I_{OUT}	—	5	8	mA	4

1. All voltages referenced to V_{SS}. All V_{DD} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns).
4. Input Voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 nanosecond set-up and hold times.

Capacitance (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, f=1MHz)

Parameter	Symbol	Test Condition	Max	Units	Notes
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF	
Data I/O Capacitance (DQ0-DQ17)	C_{OUT}	V_{OUT} = 0V	5	pF	

DC Electrical Characteristics (T_A= 0 to +70°C, V_{DD}=3.3V ± 5%)

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	I_{DD}12	—	300	mA	2, 3
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH} or CS2 = V_{IL} or $\overline{CS}$ = V_{IL} All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0 Clock @ 83MHz)	I_{SB}	—	25	mA	1, 3
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}	—	+1	µA	4
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}	—	+1	µA	
Output High Level Output “H” Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4	—	V	
Output Low Level Output “L” Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}	—	0.4	V	

1. I_{SB} = Stand-by Current.
2. I_{DD} = Selected Current.
3. I_{OUT} = Chip Output Current.
4. The input leakage current for 5.5V input is 200 µA for Clk, Chip Selects, and Output Enable. Other inputs have 100 µA of leakage current at 5.5V

AC Test Conditions (T_A=0 to +70°C, V_{DD}=3.3V ± 5%)

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V_{IH}	3.0	V	
Input Pulse Low Level	V_{IL}	0.0	V	
Input Rise Time	T_R	2.0	ns	
Input Fall Time	T_F	2.0	ns	
Input and Output Timing Reference Level		1.5	V	
Output Load Conditions				1

1. See AC Test Loading figure on page 8.

AC Characteristics (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, Units in nsec)

Parameter	Symbol	-8		-9		-10		-11		Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Cycle Time	t_{CYCLE}	12.0	—	12.0	—	12.0	—	12.0	—	
Clock Pulse High	t_{CH}	3.0	—	3.0	—	3.0	—	3.0	—	
Clock Pulse Low	t_{CL}	3.0	—	3.0	—	3.0	—	3.0	—	
Clock to Output Valid	t_{CQ}	—	8.0	—	9.0	—	10.0	—	11.0	3
Address Status Controller Setup Time	t_{ADSCS}	2.5	—	2.5	—	2.5	—	2.5	—	
Address Status Controller Hold Time	t_{ADSCH}	0.5	—	0.5	—	0.5	—	0.5	—	
Address Status Processor Setup Time	t_{ADSPS}	2.5	—	2.5	—	2.5	—	2.5	—	
Address Status Processor Hold Time	t_{ADSPH}	0.5	—	0.5	—	0.5	—	0.5	—	
Advance Setup Time	t_{ADVS}	2.5	—	2.5	—	2.5	—	2.5	—	
Advance Hold Time	t_{ADVH}	0.5	—	0.5	—	0.5	—	0.5	—	
Address Setup Time	t_{AS}	2.5	—	2.5	—	2.5	—	2.5	—	
Address Hold Time	t_{AH}	0.5	—	0.5	—	0.5	—	0.5	—	
Chip Selects Setup Time	t_{CSS}	2.5	—	2.5	—	2.5	—	2.5	—	
Chip Selects Hold Time	t_{CSH}	0.5	—	0.5	—	0.5	—	0.5	—	
Write Enables Setup Time	t_{WES}	2.5	—	2.5	—	2.5	—	2.5	—	
Write Enables Hold Time	t_{WEH}	0.5	—	0.5	—	0.5	—	0.5	—	
Data In Setup Time	t_{DS}	2.5	—	2.5	—	2.5	—	2.5	—	
Data In Hold Time	t_{DH}	0.5	—	0.5	—	0.5	—	0.5	—	
Data Out Hold Time	t_{CQX}	3.0	—	3.0	—	3.0	—	3.0	—	3
Clock High to Output High-Z	t_{CHZ}	—	5.0	—	5.0	—	5.5	—	5.5	1, 2, 4
Clock High to Output Active	t_{CLZ}	2.5	—	2.5	—	2.5	—	2.5	—	1, 2, 4
Output Enable to High-Z	t_{OHZ}	2.0	5.0	2.0	5.5	2.0	6.0	2.0	6.5	1, 4
Output Enable to Low-Z	t_{OLZ}	0.25	—	0.25	—	0.25	—	0.25	—	1, 4
Output Enable to Output Valid	t_{OQ}	—	4.0	—	5.0	—	5.0	—	6.0	3

1. Transitions are measured ± 200 mV from steady state voltage.
2. At any given voltage and temperature, T_{CHZ} (max) is always less than T_{CTZ} (min) for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from High-Z to new RAM data.
3. See AC Test Loading figure 1 on page 8.
4. See AC Test Loading figure 2 on page 8.

AC Test Loading

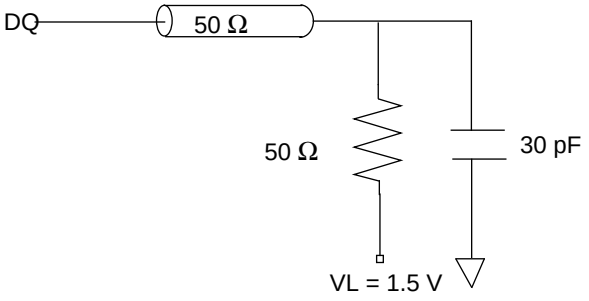


Fig. 1 Test Equivalent Load

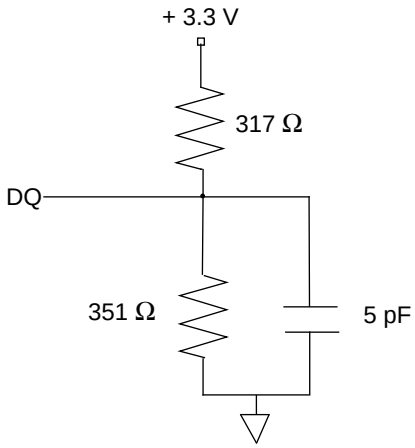
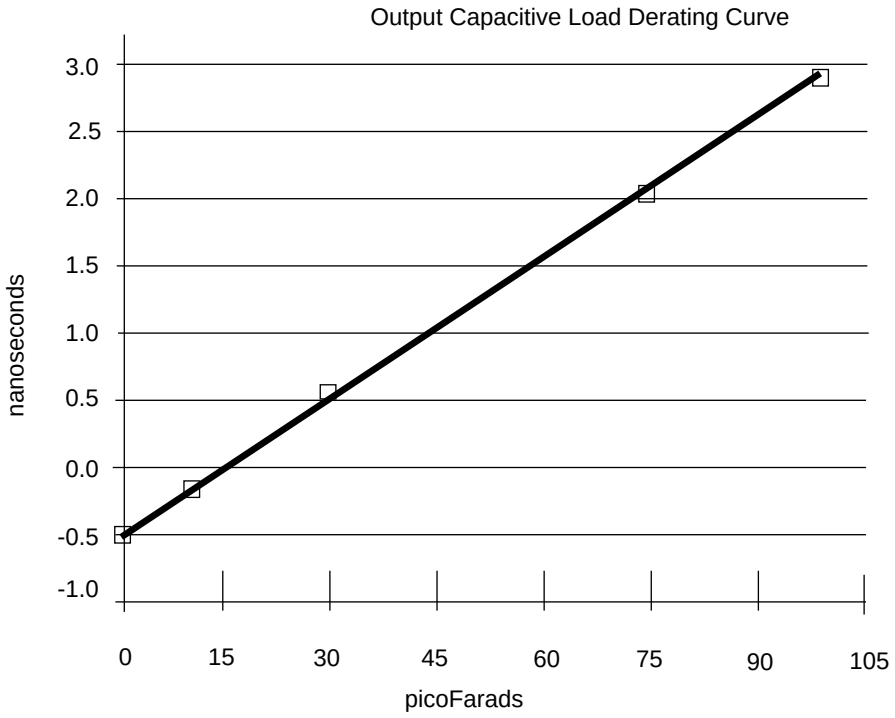
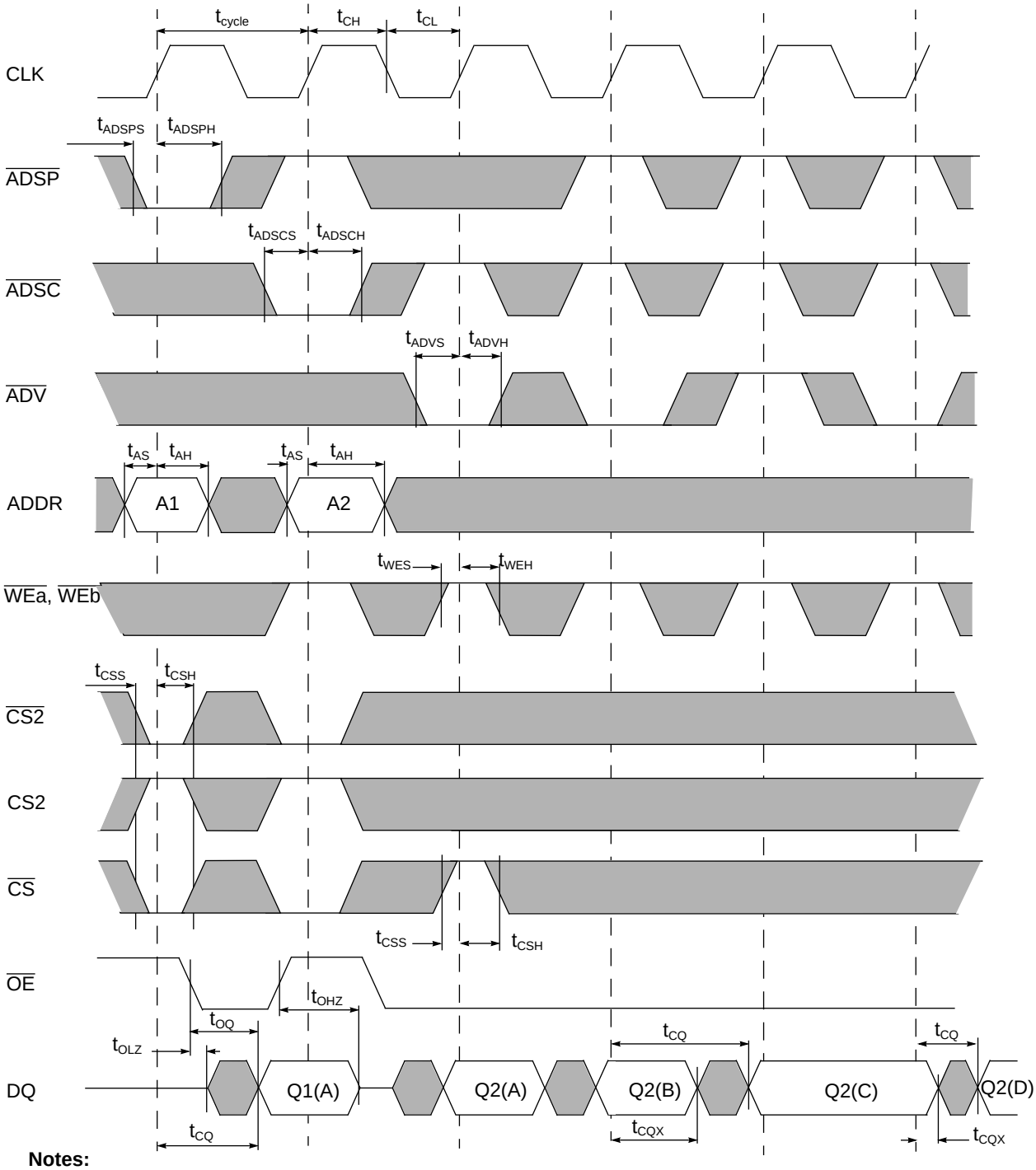


Fig. 2 Test Equivalent Load



The derating curve above is for a purely capacitive load on the output driver. For example, a part specified at 8ns access time will behave as though it has an 8.5 ns access time if a 30 pF load with no DC component was attached to the output driver. The access times guaranteed in the datasheets are based on a 50 ohm terminated test load. For unterminated loads the derating curve should be used. This curve is based on nominal process conditions with worst case parameters V_{CC} = 3.14 V, T_A = 70° C.

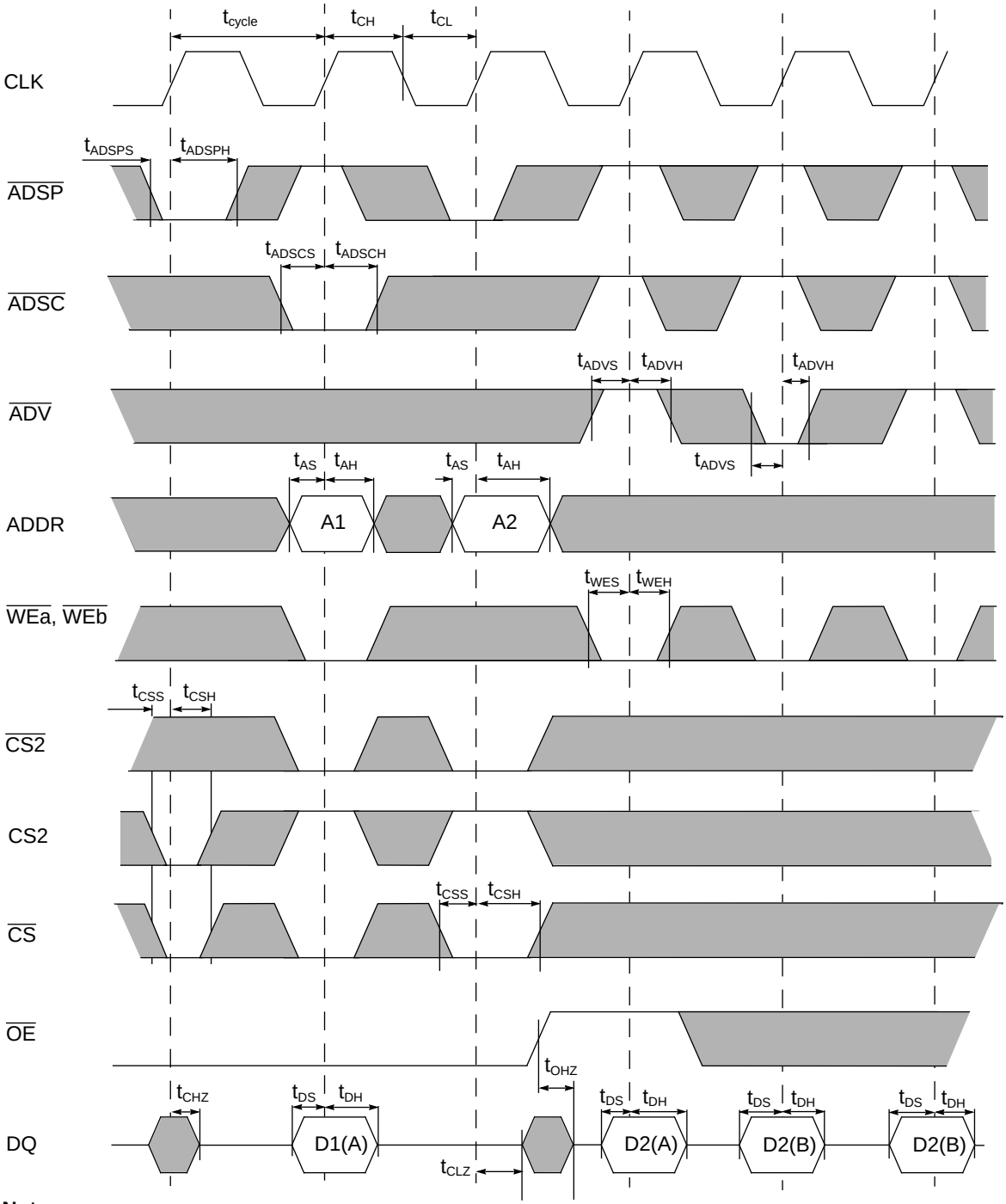
Timing Diagram (Burst Read)



Notes:

1. Q1(A) and Q2(A) refer to data written to address A1 and A2.
2. Q2(B), Q2(C) and Q2(D) refer to data written to subsequent internal burst counter addresses.

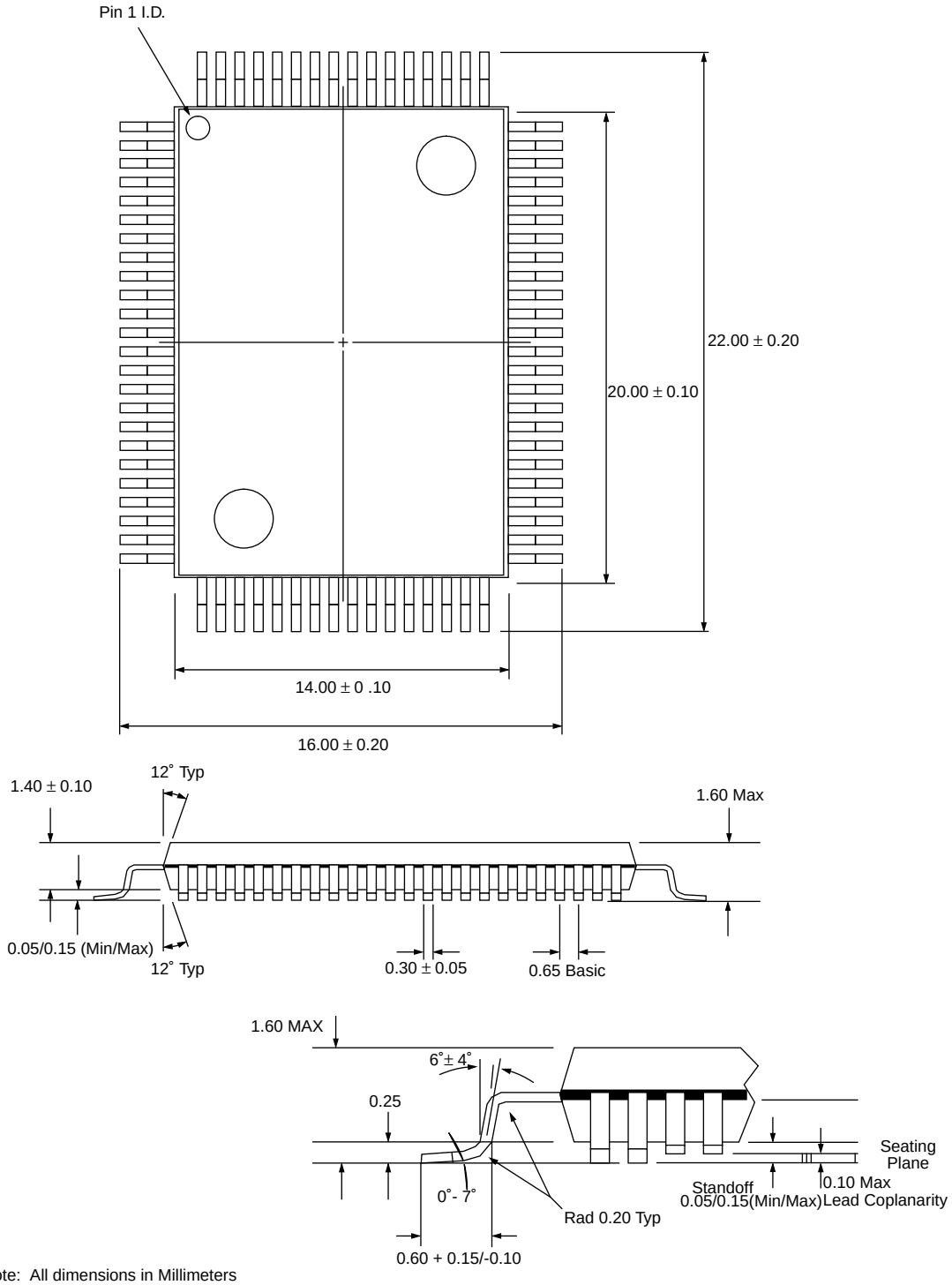
Timing Diagram (Burst Write)



Notes:

1. D1(A) and D2(A) refer to data written to address A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.
3. $\overline{WEa}$, $\overline{WEb}$ are don't cares when ADSP is sampled LOW.

100 Pin TQFP Package Diagram



Note: All dimensions in Millimeters

Connect Compatibility for 64K x18 and Future 64K x 16 & 64K x 18

TQFP PIN #	Current Connections (x18)	Future Connections (x16 & x18)	Function
4,27,54,77	NC	V_{DDQ}	Output Power Supply
5,26,55,76	NC	V_{SS}	Ground
14	NC	Low or High, NC for most vendors but Low or High to comply to the JEDEC standard.	$\overline{FT}$, FLow thru or Pipeline function, tie Low for flow thru, High for Pipeline
24	DQP2	NC or DQ in x18	Parity bit for second byte
31	NC	Low or High	$\overline{LBO}$, Linear Burst Order, This pin must be tied low for linear(PowerPC), High for Interleave (Pentium)
64	NC	Low or High. Low allows normal operation.	ZZ , Asynchronous Sleep Mode, Tie to ground for normal function, V_{DDQ} for sleep mode (Low power state)
74	DQP1	NC or DQ in x18	Parity bit for first byte
87	NC	Low or $\overline{BWE}$, Tie low if function not used	Byte Write Enable, Allows individual bytes to be written.
88	NC	Low or $\overline{GW}$, Tie High if function not used	Global Write Enable, Allows write of all bytes to occur with single pin.

The IBM041812PQK has the pins connected in the manner indicated in the Current Connections (x18) and is also JEDEC complaint. Future Connections refers to the evolution on the JEDEC standard for subsequent part numbers.

Revision Log

Rev	Contents of Modification
7/95	Initial Release of the 64K x 18 (8/9/10/11) TQFP BURST MODE Application Spec.

For more information contact your IBM Microelectronics sales representative or
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Integrated Device Technology, Inc.

BiCMOS StaticRAM 240K (16K x 15-BIT) CACHE-TAG RAM For PowerPC™ and RISC Processors

IDT71216

FEATURES:

- 16K x 15 Configuration
  - 12 TAG Bits
  - 3 Separate I/O Status Bits (Valid, Dirty, Write Through)
- Match output uses Valid bit to qualify MATCH output
- High-Speed Address-to-Match comparison times
  - 8/9/10/12ns over commercial temperature range
- $\overline{TA}$ circuitry included inside the Cache-Tag for highest speed operation
- Asynchronous Read/Match operation with Synchronous Write and Reset operation
- Separate $\overline{WE}$ for the TAG bits and the Status bits
- Separate $\overline{OE}$ for the TAG bits, the Status bits, and $\overline{TA}$
- Synchronous $\overline{RESET}$ pin for invalidation of all Tag entries
- Dual Chip selects for easy depth expansion with no performance degredation
- I/O pins both 5V TTL and 3.3V LVTTL compatible with V_{CCQ} pins
- $\overline{PWRDN}$ pin to place device in low-power mode
- Packaged in a 80-pin Thin Plastic Quad Flat Pack (TQFP)

DESCRIPTION:

The IDT71216 is a 245,760-bit Cache Tag StaticRAM, organized 16K x 15 and designed to support PowerPC and other RISC processors at bus speeds up to 66MHz. There are twelve common I/O TAG bits, with the remaining three bits used as status bits. A 12-bit comparator is on-chip to allow fast comparison of the twelve stored TAG bits and the current Tag input data. An active HIGH MATCH output is generated when these two groups of data are the same for a given address. This high-speed MATCH signal, with t_{ADM} as fast as 8ns, provides the fastest possible enabling of secondary cache accesses.

The three separate I/O status bits (VLD, DTY, and WT) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC LOW, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given Tag data. SFUNC HIGH releases the defined internal status bit usage and control, allowing the user to configure the status bit information to fit his system needs. A synchronous $\overline{RESET}$ pin, when held LOW at a rising clock edge, will reset all status bits in the array for easy invalidation of all Tag addresses.

The IDT71216 also provides the option for Transfer Acknowledge ($\overline{TA}$) generation within the cache tag itself, based upon MATCH, VLD bit, WT bit, and external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and Read operations are both asynchronous in order to provide the fastest access times possible, while Write operations are synchronous for ease of system timing.

The IDT71216 uses a 5V power supply on Vcc, with separate V_{CCQ} pins provided for the outputs to offer compliance with both 5.0V TTL and 3.3V LVTTL Logic levels. The $\overline{PWRDN}$ pin offers a low-power standby mode to reduce power consumption by 90%, providing significant system power savings.

The IDT71216 is fabricated using IDT's high-performance, high-reliability BiCMOS technology and is offered in a space-saving 80-pin Thin Plastic Quad Flat Pack (TQFP) package.

PIN DESCRIPTIONS

$A_0 – A_{13}$	Address Inputs	Input
$\overline{CS1}$, CS2	Chip Selects	Input
$\overline{WET}$	Write Enable - Tag Bits	Input
$\overline{WES}$	Write Enable - Status Bits	Input
$\overline{OET}$	Output Enable - Tag Bits	Input
$\overline{OES}$	Output Enable - Status Bits	Input
$\overline{RESET}$	Status Bit Reset	Input
$\overline{PWRDN}$	Powerdown Mode Control Pin	Input
SFUNC	Status Bit Function Control Pin	Input
TT1	Read/Write Input from Processor	Input
VLD_{IN} / S_{1IN}	Valid Bit / S_1 Bit Input	Input
DTY_{IN} / S_{2IN}	Dirty Bit / S_2 Bit Input	Input
WT_{IN} / S_{3IN}	Write Through Bit / S_3 Bit Input	Input

CLK	System Clock	Input
TAH	$\overline{TA}$ Force High	Input
$\overline{TAOE}$	$\overline{TA}$ Output Enable	Input
$\overline{TAIN}$	Additional $\overline{TA}$ Input	Input
$\overline{TA}$	Transfer Acknowledge	Output
$TAG_0 – TAG_{11}$	Tag Data Input/Outputs	I/O
VLD_{OUT} / S_{1OUT}	Valid Bit / S_1 Bit Output	Output
DTY_{OUT} / S_{2OUT}	Dirty Bit / S_2 Bit Output	Output
WT_{OUT} / S_{3OUT}	Write Through Bit / S_3 Bit Output	Output
MATCH	Match	Output
V_{CC}	+5V Power	Pwr
V_{CCQ}	Output Buffer Power	QPwr
V_{SS}	Ground	Gnd

3067 tbl 01

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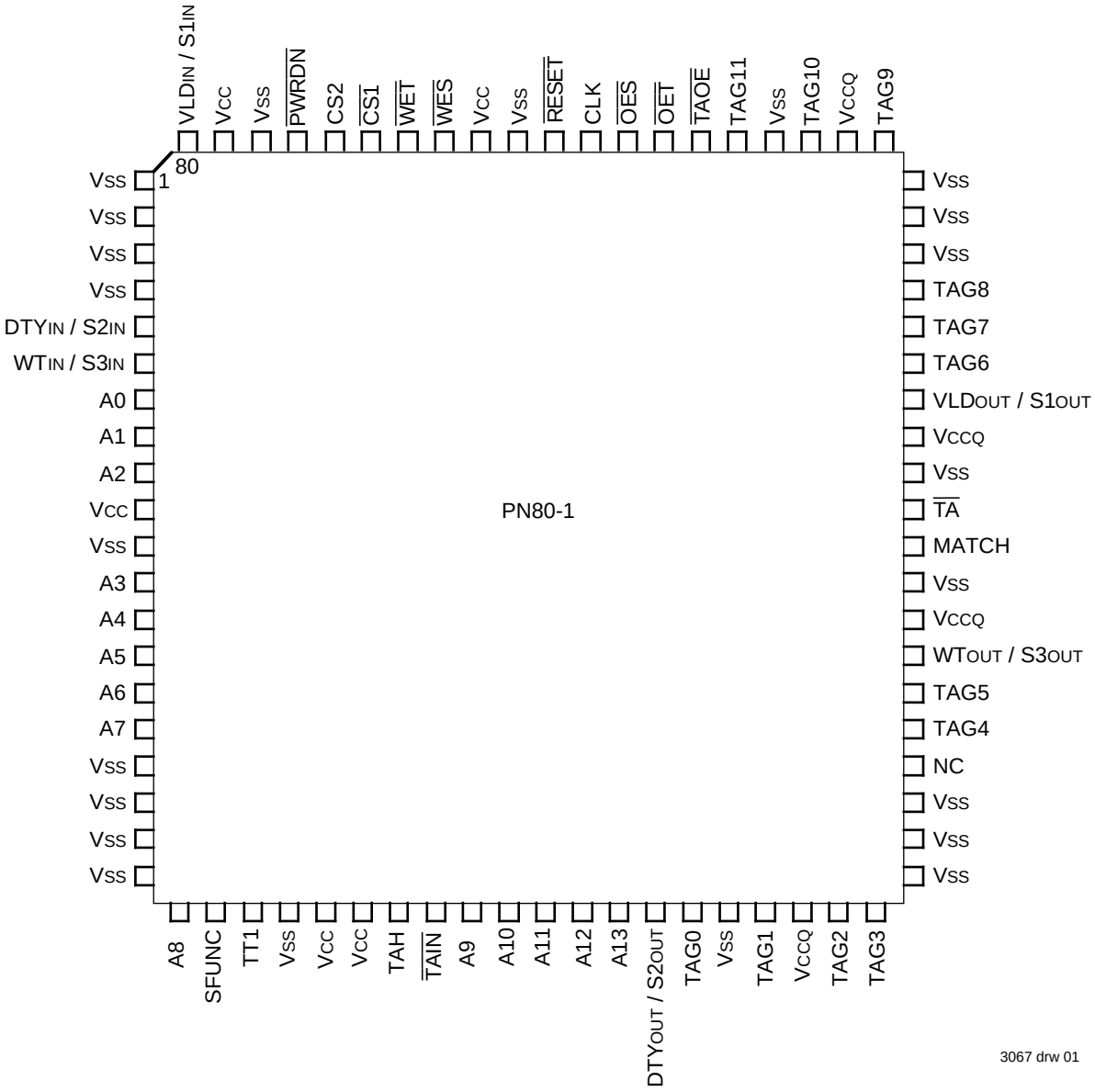
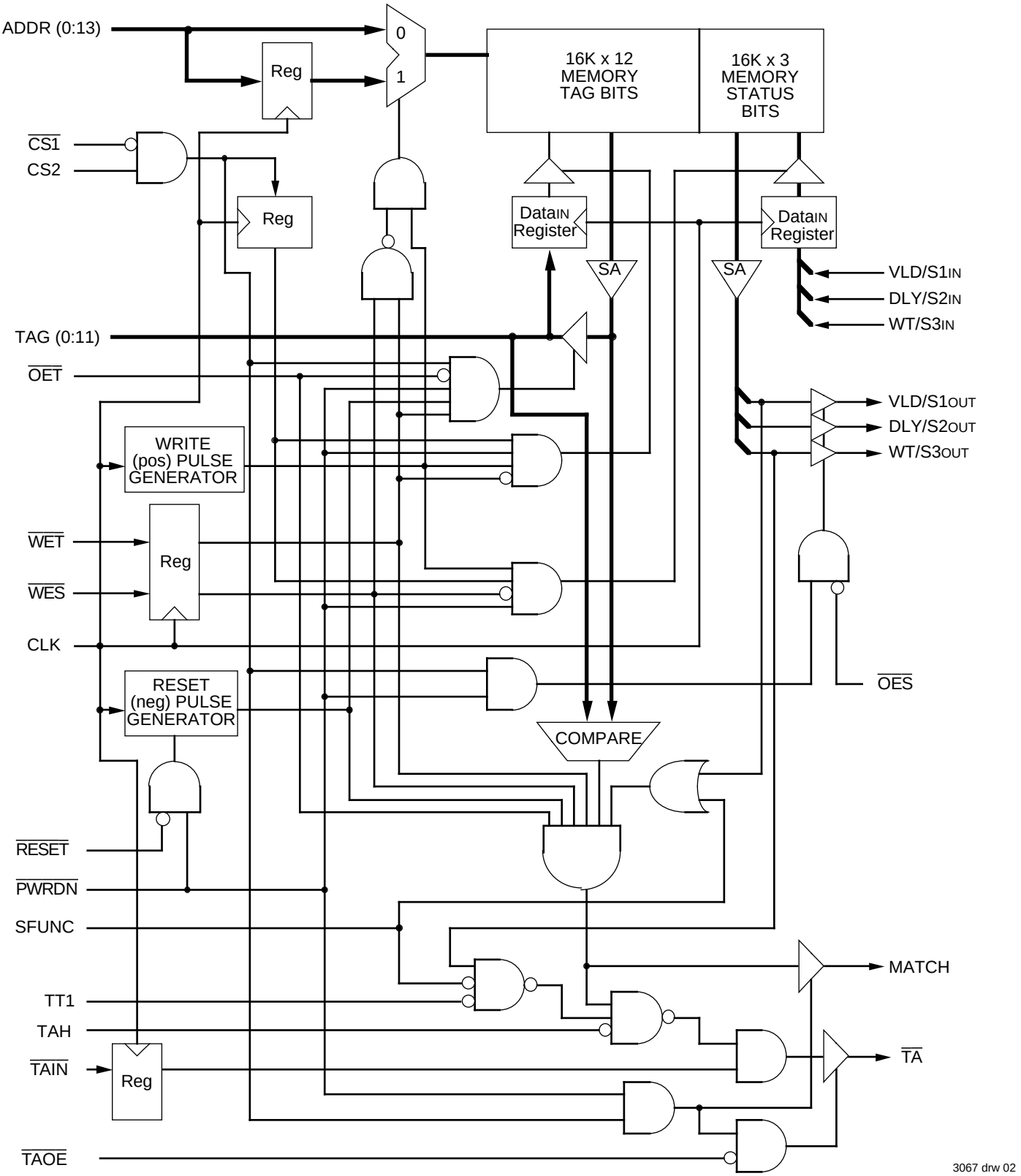
PowerPC is a trademark of International Business Machines, Inc.

PIN CONFIGURATION



TQFP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

CHIP SELECT, RESET, AND POWER-DOWN FUNCTIONS(1, 2)

$\overline{CS1}$	CS2	$\overline{RESET}$	$\overline{PWRDN}$	CLK	$\overline{WET}$	$\overline{WES}$	$\overline{TAOE}$		TAG	VLD_{OUT}	DTY_{OUT}	WT_{OUT}	MATCH	$\overline{TA}$	OPERATION	POWER
CHIP SELECT FUNCTION																
H	X	X	H	X	X	X	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
X	L	X	H	X	X	X	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
L	H	X	H	X	X	X	X		–	–	–	–	–	–	Selected	Active
RESET FUNCTION																
L	H	L	H	↑	H	H	L		Hi-Z	L(3)	L(3)	L(3)	L(3)	H	Reset Status	Active
L	H	L	H	↑	H	H	H		Hi-Z	L(3)	L(3)	L(3)	L(3)	Hi-Z	Reset Status	Active
H	X	L	H	↑	H	H	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	L	L	H	↑	H	H	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	X	L	H	↑	L	X	X		–	–	–	–	–	–	Not Allowed	–
X	X	L	H	↑	X	L	X		–	–	–	–	–	–	Not Allowed	–
POWER-DOWN FUNCTION																
X	X	X	L	X	H	H	X		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power-down	Standby

NOTES: 3067 tbl 02

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. $\overline{OET}$, $\overline{OES}$, TT1, TAH, $\overline{TAIN}$ and SFUNC are "X" for this table.
3. $\overline{OES}$ is LOW.

READ AND WRITE FUNCTIONS(1, 2)

$\overline{OET}$	$\overline{OES}$	$\overline{WET}$	$\overline{WES}$	CLK	TT1		TAG	VLD_{IN}	DTY_{IN}	WT_{IN}	VLD_{OUT}	DTY_{OUT}	WT_{OUT}	MATCH	OPERATION
READ FUNCTION															
L	X	H	X	X	X		D_{OUT}	–	–	–	–	–	–	D_{OUT}	Read TAG I/O
X	L	X	X	X	X		–	–	–	–	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Read Status Bits
H	X	X	X	X	X		Hi-Z	–	–	–	–	–	–	D_{OUT}	TAG I/O Disable
X	H	X	X	X	X		–	–	–	–	Hi-Z	Hi-Z	Hi-Z	D_{OUT}	Status Disabled
WRITE FUNCTION															
H	X	L	X	↑	X		D_{IN}	–	–	–	D_{OUT}	D_{OUT}	D_{OUT}	L	Write TAG I/O
L	X	L	X	↑	X		–	–	–	–	–	–	–	–	Not Allowed
X	L	X	L	↑	X		–	D_{IN}	D_{IN}	D_{IN}	D_{OUT}(3)	D_{OUT}(3)	D_{OUT}(3)	L	Write Status Bits
X	H	X	L	↑	X		–	D_{IN}	D_{IN}	D_{IN}	Hi-Z	Hi-Z	Hi-Z	L	Write Status Bits

NOTES: 3067 tbl 03

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. This table applies when $\overline{CS1}$ is LOW and CS2, $\overline{RESET}$, and $\overline{PWRDN}$ are HIGH. $\overline{TAOE}$, TAH, $\overline{TAIN}$ and SFUNC are "X" for this table.
3. D_{OUT} in this case is the same as DIN; that is, the input data is written through to the outputs during the write operation.

TRUTH TABLES (CONT.)

MATCH FUNCTION(1, 2, 3)

$\overline{CS1}$	CS2	SFUNC	$\overline{OET}$	$\overline{WET}$	$\overline{WES}$	TAG	VLD(4)	DTY(4)	WT(4)	MATCH	OPERATION
H	X	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
X	L	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
L	H	X	X	X	X	–	–	–	–	DOUT	Selected
L	H	X	L	H	X	DOUT	–	–	–	L	Read Tag I/O
L	H	X	H	L	X	DIN	–	–	–	L	Write Tag I/O
L	H	X	X	X	L	–	DIN	DIN	DIN	L	Write Status Bits
L	H	L	H	H	H	TAGIN	L	–	–	L	Invalid Data - Dedicated Status Bits
L	H	L	H	H	H	TAGIN	H	–	–	M	Match - Dedicated Status Bits
L	H	H	H	H	H	TAGIN	X	–	–	M	Match - Generic Status Bits

NOTES: 3067 tbl 04

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are HIGH for this table. TT1, TAH, $\overline{TAOE}$, $\overline{TAIN}$, $\overline{OES}$, and CLK are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.

$\overline{TA}$ FUNCTION(1, 2, 3, 5)

$\overline{TAOE}$	$\overline{TAIN}$(6)	$\overline{OET}$	$\overline{WET}$	$\overline{WES}$	TAH	TT1	SFUNC	VLD(4)	DTY(4)	WT(4)	TAG	MATCH	$\overline{TA}$	OPERATION
H	X	X	X	X	X	X	X	X	–	X	–	–	Hi-Z	$\overline{TA}$ Disabled
L	L	X	X	X	X	X	X	X	–	X	–	X	L	External $\overline{TA}$ Input (7)
L	H	L	X	X	X	X	X	X	–	X	DOUT	L	H	Read TAG
L	H	X	L	X	X	X	X	X	–	X	DIN	L	H	Write TAG
L	H	X	X	L	X	X	X	DIN	DIN	DIN	–	L	H	Write Status
L	H	X	X	X	H	X	X	X	–	X	–	X	H	Force $\overline{TA}$ HIGH
L	H	X	X	X	X	X	L	L	–	X	–	L	H	Invalid TAG
L	H	X	X	X	X	L	L	X	–	H	–	X	H	Write Through
L	H	H	H	H	L	X	L	H	–	L	TAGIN	M	$\overline{M}$	Compare
L	H	H	H	H	L	H	L	H	–	X	TAGIN	M	$\overline{M}$	Compare
L	H	H	H	H	L	X	L	H	–	X	TAGIN	M	$\overline{M}$	Compare
L	H	H	H	H	L	X	H	X	–	X	TAGIN	M	$\overline{M}$	Compare

NOTES: 3067 tbl 05

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
3. $\overline{PWRDN}$ and $\overline{RESET}$ are HIGH for this table. CLK and $\overline{OES}$ are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.
5. $\overline{CS1}$ is LOW, CS2 is HIGH for this table.
6. $\overline{TAIN}$ is a synchronous input; thus the inputs noted in the table must be applied during a rising CLK edge.
7. $\overline{TAIN}$ will be a factor in determining the $\overline{TA}$ output in all cases except when TAH is HIGH and there is a valid MATCH. In that case, $\overline{TA}$ will be LOW(Valid).

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{CCQ}	5V Output Buffers	4.75	5.0	5.25	V
V_{CCQ}	3.3V Output Buffers	3.0	3.3	3.6	V
V_{SS}	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.0	VCC+0.3	V
V_{IHQ}	I/O High Voltage	2.2	3.0	VCCQ+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3067 tbl 06

1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{TAG}	TAG Input/Output Capacitance	$V_{I/O}$ = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3067 tbl 07

1. This parameter is determined by device characterization but is not production tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0(2)	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.7	W
I_{OUT}	DC Output Current	20	mA

NOTES: 3067 tbl 08

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{IN} should not exceed Vcc+0.5V. All pins should not exceed 7.0V. V_{CCQ} should never exceed V_{CC}, and V_{CC} should never exceed V_{CCQ} + 4.0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS1} \geq V_{IH}$, CS2 ≤ V_{IL}, $\overline{OE} \geq V_{IH}$, V_{CC} = Max. V_{OUT} = 0V to V_{CCQ}, V_{CCQ} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3067 tbl 09

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1, 2) (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	71216S8		71216S9		71216S10		71216S12		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Operating Power Supply Current	$\overline{PWRDN} \geq V_{IH}$ Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	330	—	300	—	290	—	280	—	mA
I_{SB}	Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{IH}$ or ≤ V_{IL} V_{CC} = Max., f = f_{MAX}(3)	30	—	30	—	30	—	30	—	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{HC}$ or ≤ V_{LC}(4) V_{CC} = Max., f = 0(3)	25	—	25	—	25	—	25	—	mA

NOTES: 3067 tbl 10

1. All values are maximum guaranteed values.
2. $\overline{CS1} \leq V_{IL}$, CS2 ≥ V_{IH}.
3. f_{MAX} =1/t_{CYC} (all address inputs are cycling at f_{MAX}). f = 0 means no address input lines are changing.
4. V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{AAT}	Address Access Time Tag Bits	—	10	—	11	—	12	—	14	ns
t_{ACST}	Chip Select Access Time Tag Bits	—	8	—	9	—	10	—	12	ns
t_{CLZ}(1)	Chip Select to Tag and Status Bits in Low-Z	1	—	1	—	1	—	1	—	ns
t_{CHZ}(1)	Chip Select to Tag and Status Bits in High-Z	1	5	1	6	1	6	1	7	ns
t_{OET}	Output Enable to Tag Bits Valid	—	5	—	6	—	6	—	7	ns
t_{OTLZ}(1)	Output Enable to Tag Bits in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OTHZ}(1)	Output Enable to Tag Bits in High-Z	1	5	1	6	1	6	1	7	ns
t_{TOH}	Tag Bit Hold from Address Change	2	—	2	—	2	—	2	—	ns
t_{OES}	Output Enable to Status Bits Valid	—	5	—	6	—	6	—	7	ns
t_{OSLZ}(1)	Output Enable to Status Bits in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OSHZ}(1)	Output Enable to Status Bits in High-Z	1	5	1	6	1	6	1	7	ns
t_{AAS}	Address Access Time Status Bits	—	8	—	9	—	10	—	12	ns
t_{ACSS}	Chip Select Access Time Status Bits	—	6	—	7	—	8	—	10	ns
t_{SOH}	Status Bit Hold from Address Change	2	—	2	—	2	—	2	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3067 tbl 11

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset and Power Down Cycles										
t_{SR}	$\overline{RESET}$ Set-up Time	4	—	4	—	4	—	4	—	ns
t_{HR}	$\overline{RESET}$ Hold Time	1	—	1	—	1	—	1	—	ns
t_{SRST}	Status Bit Reset Time	—	50	—	60	—	60	—	70	ns
t_{SHRS}	Status Bit Hold from $\overline{RESET}$ LOW	2	—	2	—	2	—	2	—	ns
t_{RSMI}	$\overline{RESET}$ LOW to MATCH and $\overline{TA}$ Invalid	—	9	—	10	—	10	—	12	ns
t_{RSMV}	$\overline{RESET}$ HIGH to MATCH and $\overline{TA}$ Valid	—	110	—	120	—	120	—	130	ns
t_{RSHZ}(2)	$\overline{RESET}$ LOW to TAG High-Z	—	9	—	10	—	10	—	12	ns
t_{RSLZ}(2)	$\overline{RESET}$ HIGH to TAG Low-Z	—	90	—	100	—	100	—	110	ns
t_{PDSR}	$\overline{PWRDN}$ Set-up to $\overline{RESET}$ LOW	30	—	30	—	30	—	30	—	ns
t_{RHPL}	$\overline{RESET}$ HIGH to $\overline{PWDRN}$ LOW	1	—	1	—	1	—	1	—	CLK
t_{RHWL}	$\overline{RESET}$ HIGH to $\overline{WET}$ and $\overline{WES}$ LOW	90	—	95	—	95	—	105	—	ns
t_{PD}(2)	$\overline{PWRDN}$ LOW to Low Power Mode	—	50	—	50	—	50	—	50	ns
t_{PU}(2)	$\overline{PWRDN}$ HIGH to Active Power Mode	0	—	0	—	0	—	0	—	ns
t_{PDHZ}(2)	$\overline{PWRDN}$ LOW to Outputs in High-Z	—	9	—	10	—	10	—	12	ns
t_{PDLZ}(2)	$\overline{PWRDN}$ HIGH to Outputs in Low-Z	0	—	0	—	0	—	0	—	ns
t_{PUV}	$\overline{PWRDN}$ HIGH to Outputs Valid	—	50	—	50	—	50	—	50	ns
t_{WHPL}(2)	$\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW	5	—	5	—	5	—	5	—	ns
t_{PUWL}	$\overline{PWRDN}$ HIGH to $\overline{WET}$ and $\overline{WES}$ Active	50	—	50	—	50	—	50	—	ns

NOTES:
1. Power-down mode is intended to be used during extended time periods of device inactivity.
2. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3067 tbl 12

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle and Clock Parameters										
t_{CYC}	Clock Cycle Time	15	—	15	—	15	—	16.6	—	ns
t_{CH}(2, 3)	Clock Pulse HIGH	4.5	—	4.5	—	4.5	—	5	—	ns
t_{CL}(2, 3)	Clock Pulse LOW	4.5	—	4.5	—	4.5	—	5	—	ns
t_S	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Set-up Time	3	—	3	—	3	—	3	—	ns
t_H	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Hold Time	1	—	1	—	1	—	1	—	ns
t_{SA}	Address Set-up Time	3	—	3	—	3	—	3	—	ns
t_{HA}	Address Hold Time	1	—	1	—	1	—	1	—	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{TA}$ Invalid	—	6	—	7	—	7	—	8	ns
t_{CKLZ}(3)	CLK HIGH Read to Outputs in Low-Z	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{CTV}(4)	CLK HIGH Read to Tag Bits Valid	—	9	—	10	—	10	—	12	ns
t_{CSV}(4)	CLK HIGH Write to Status Outputs Valid	—	8	—	9	—	9	—	10	ns
t_{CSH}(3)	Status Output Hold from CLK HIGH Write	0	—	0	—	0	—	0	—	ns
t_{WHPL}	$\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW	5	—	5	—	5	—	5	—	ns
t_{PUWL}	PWRDN HIGH to WET and WES Active	50	—	50	—	50	—	50	—	ns

NOTES: 3067 tbl 14

1. All Write cycles are synchronous and referenced from rising CLK.
2. This parameter is measured as a HIGH time above 2.0V and a LOW time below 0.8V.
3. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
4. Addresses are stable prior to CLK transition HIGH.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S8		IDT71216S9		IDT71216S10		IDT71216S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
MATCH and $\overline{TA}$ Cycles										
t_{ADM}	Address to MATCH Valid	—	8	—	9	—	10	—	12	ns
t_{DAM}	Data Input to MATCH Valid	—	8	—	9	—	10	—	12	ns
t_{CSM}	Chip Select to MATCH Valid	—	8	—	9	—	10	—	12	ns
t_{CMLZ}(1)	Chip Select to MATCH in Low-Z	1	—	1	—	1	—	1	—	ns
t_{CMHZ}(1)	Chip Select to MATCH in High-Z	1	5	1	6	1	6	1	7	ns
t_{MHA}	MATCH Valid Hold from Address	2	—	2	—	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold from Data	2	—	2	—	2	—	2	—	ns
t_{BHA}	$\overline{TA}$ Valid Hold from Address	2	—	2	—	2	—	2	—	ns
t_{BHD}	$\overline{TA}$ Valid Hold from Data	2	—	2	—	2	—	2	—	ns
t_{ADB}	Address to $\overline{TA}$ Valid	—	9	—	10	—	11	—	13	ns
t_{DAB}	Data Input to $\overline{TA}$ Valid	—	9	—	10	—	11	—	13	ns
t_{CSB}	Chip Select LOW to $\overline{TA}$ Valid	—	9	—	10	—	11	—	13	ns
t_{OEBV}	$\overline{TAOE}$ LOW to $\overline{TA}$ Valid	—	6	—	6	—	7	—	8	ns
t_{OBLZ}(1)	$\overline{TAOE}$ LOW to $\overline{TA}$ in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OBHZ}(1)	$\overline{TAOE}$ HIGH to $\overline{TA}$ in High-Z	1	5	1	6	1	6	1	7	ns
t_{BYFH}	TAH HIGH to Force $\overline{TA}$ HIGH	—	5	—	5	—	5	—	6	ns
t_{BYHV}	TAH LOW to $\overline{TA}$ Valid	—	5	—	5	—	5	—	6	ns
t_{SB}	$\overline{TAIN}$ Set-up Time	4	—	4	—	4	—	4	—	ns
t_{HB}	$\overline{TAIN}$ Hold Time	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{BIBL}	CLK HIGH $\overline{TAIN}$ LOW to $\overline{TA}$ LOW	—	6	—	6	—	7	—	8	ns
t_{BIBV}	CLK HIGH $\overline{TAIN}$ HIGH to $\overline{TA}$ Valid	—	6	—	6	—	7	—	8	ns
t_{OEMI}	$\overline{OET}$ LOW to MATCH and $\overline{TA}$ Invalid	—	6	—	7	—	7	—	8	ns
t_{OEMV}	$\overline{OET}$ HIGH to MATCH and $\overline{TA}$ Valid	—	7	—	8	—	8	—	10	ns
t_{WRBH}(2)	W/$\overline{R}$ HIGH to $\overline{TA}$ HIGH	—	6	—	7	—	7	—	8	ns
t_{WRBV}(2)	W/$\overline{R}$ LOW to $\overline{TA}$ Valid	—	6	—	7	—	7	—	8	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{TA}$ Invalid	—	7	—	7	—	7	—	8	ns
t_{WMV}(3)	CLK HIGH Read to MATCH and $\overline{TA}$ Valid	—	8	—	9	—	10	—	12	ns

NOTES:

3067 tbl 15

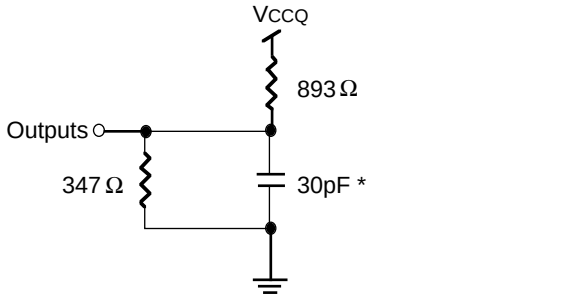
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
2. These parameters only apply when SFUNC is LOW and the internal WT bit is HIGH.
3. t_{ADM}, t_{DAM}, t_{CSM} and t_{ADB}, t_{DAB}, t_{CSB} must also be satisfied.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figs. 1, 2, 3, & 4

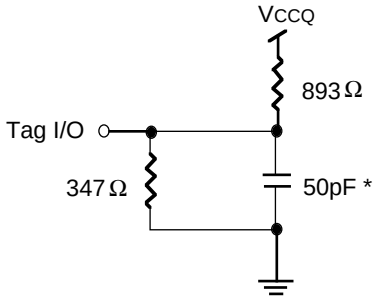
3067 tbl 16

AC TEST LOADS



3067 drw 03

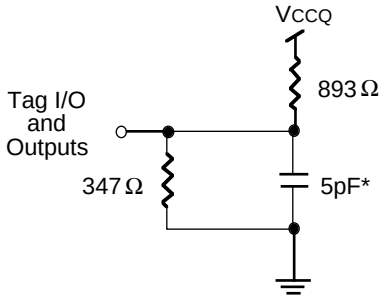
Figure 1. AC Test Load



3067 drw 04

Figure 2. Tag I/O AC Test Load

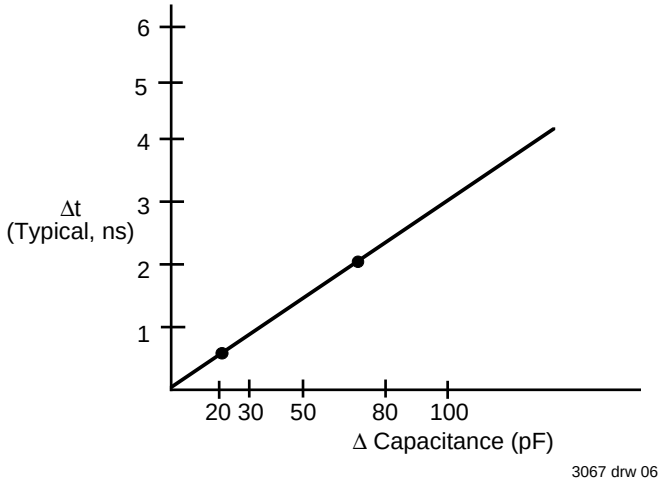
*** Including scope and jig capacitance**



3067 drw 05

Figure 3. AC Test Load (for t_{HZ} and t_{LZ} parameters)

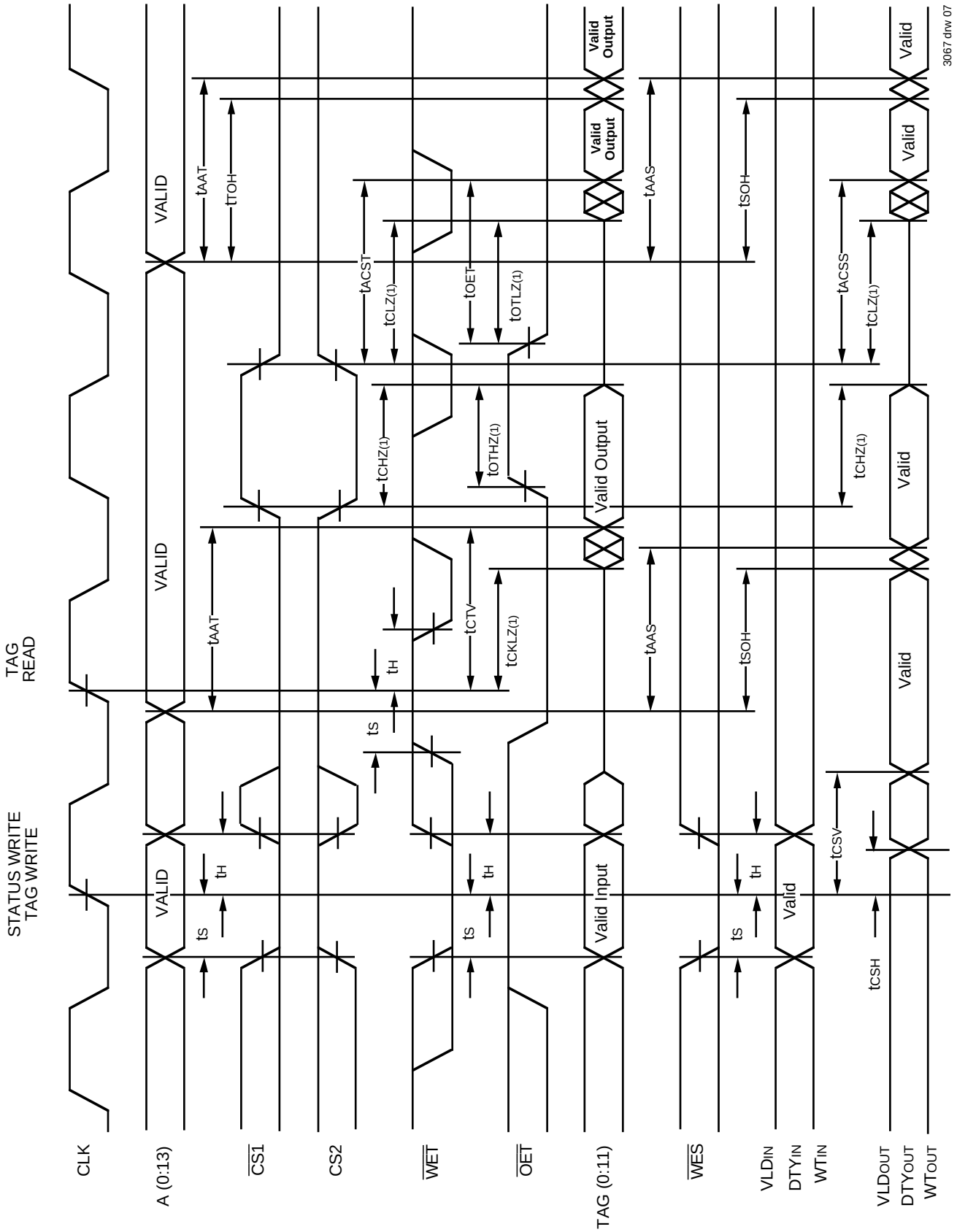
*** Including scope and jig capacitance**



3067 drw 06

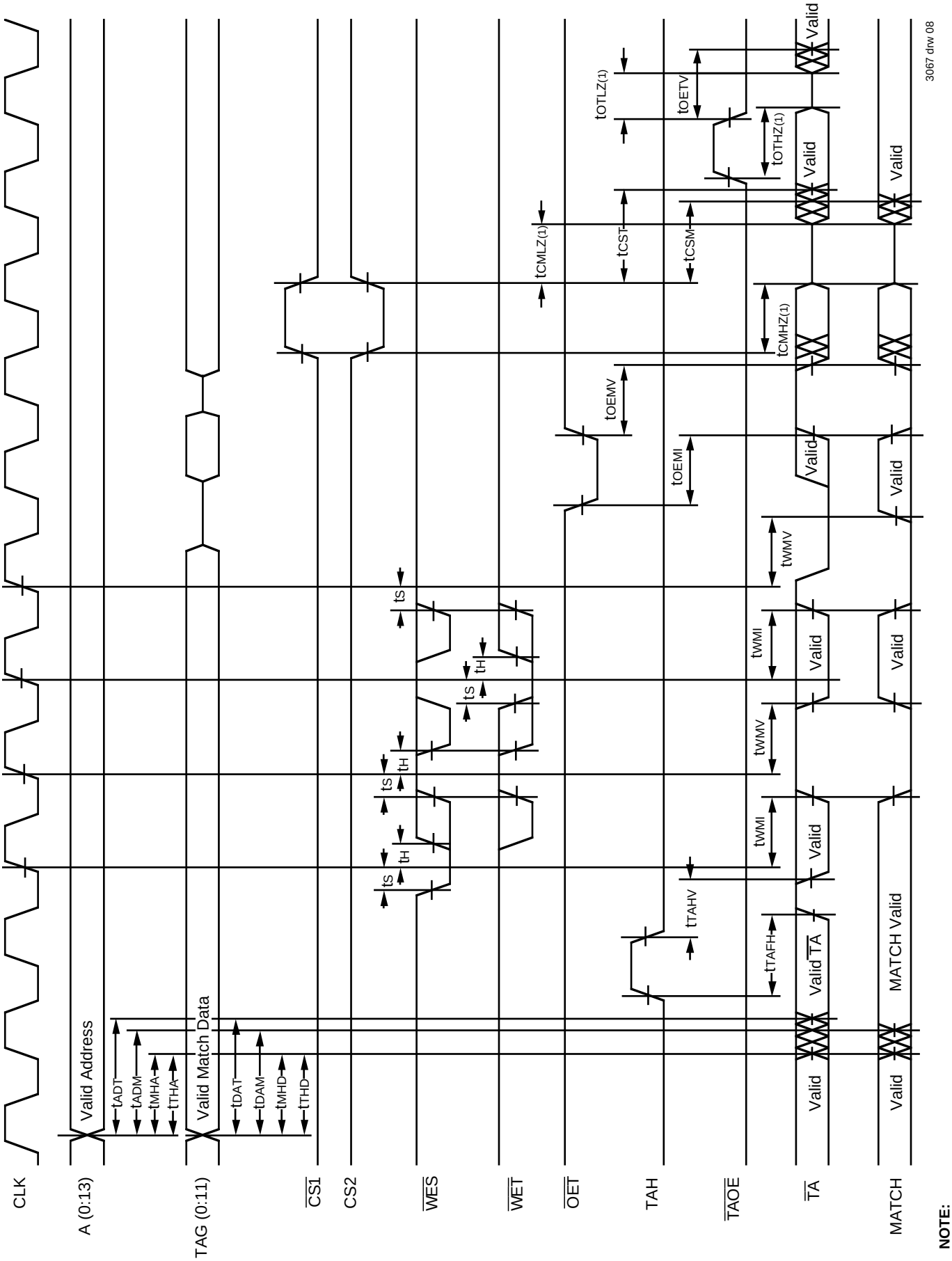
Figure 4. Lumped Capacitance Load, Typical Derating

TIMING WAVEFORMS OF WRITE AND READ CYCLES



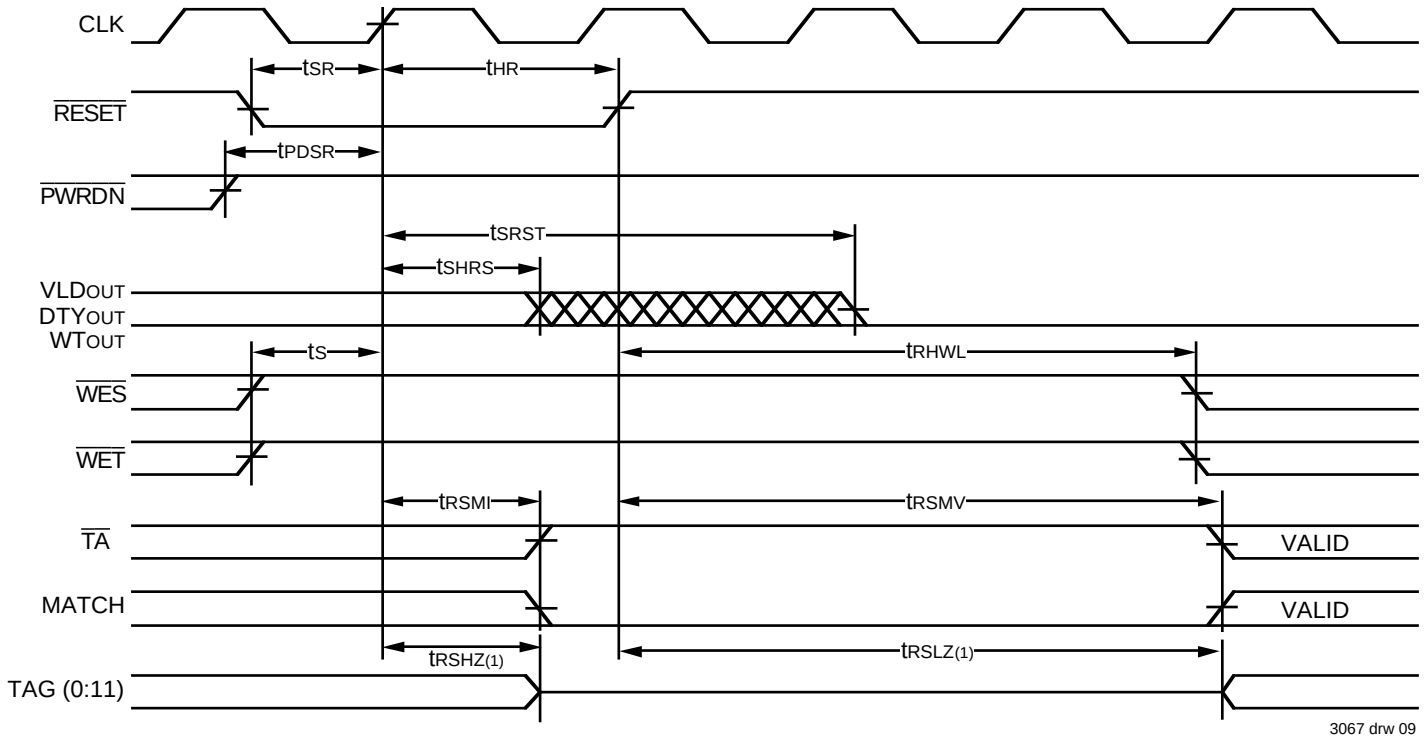
NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF MATCH AND $\overline{TA}$ FUNCTIONS



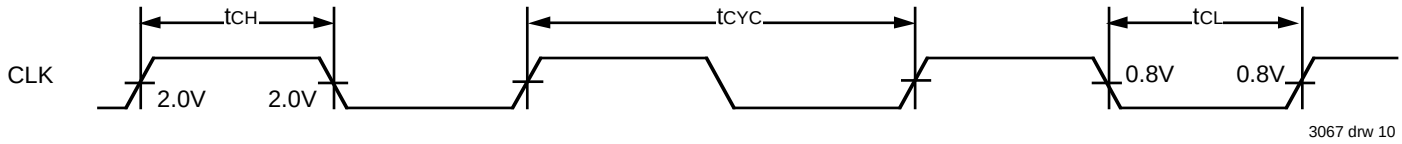
NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF $\overline{\text{RESET}}$ FUNCTION



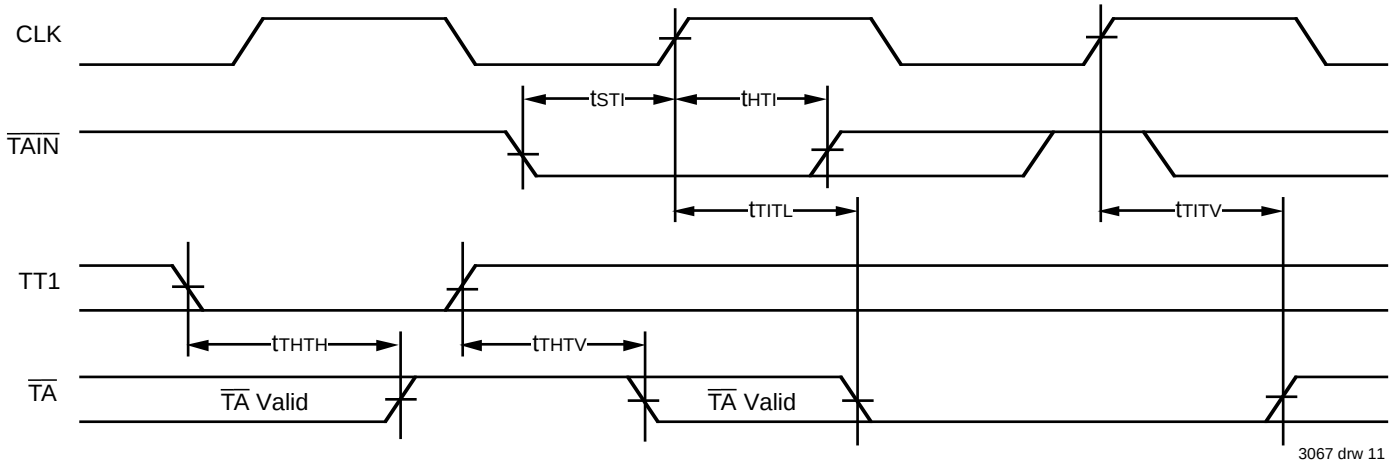
NOTE:
1. Transition is measured ±200mV from steady state.

CLOCK TIMING WAVEFORM

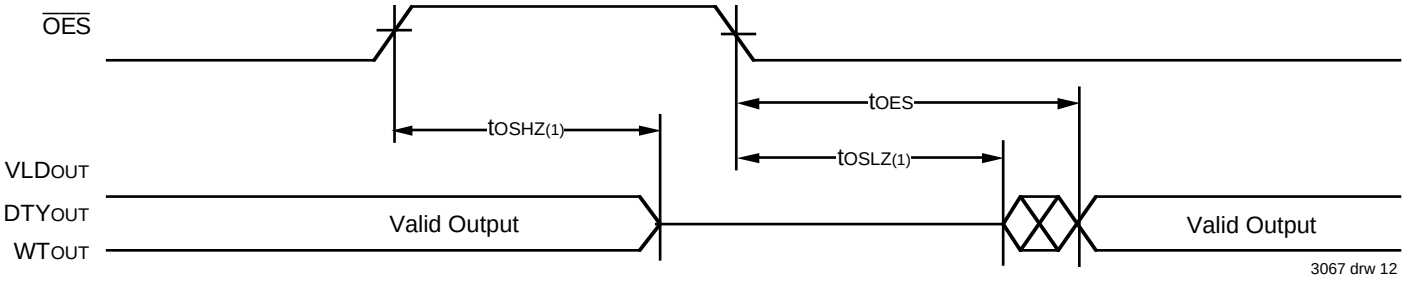


TIMING WAVEFORMS OF $\overline{\text{TA}}$ AND TT1 SIGNAL

Applies when SFUNC is LOW, and the internal WT bit is HIGH

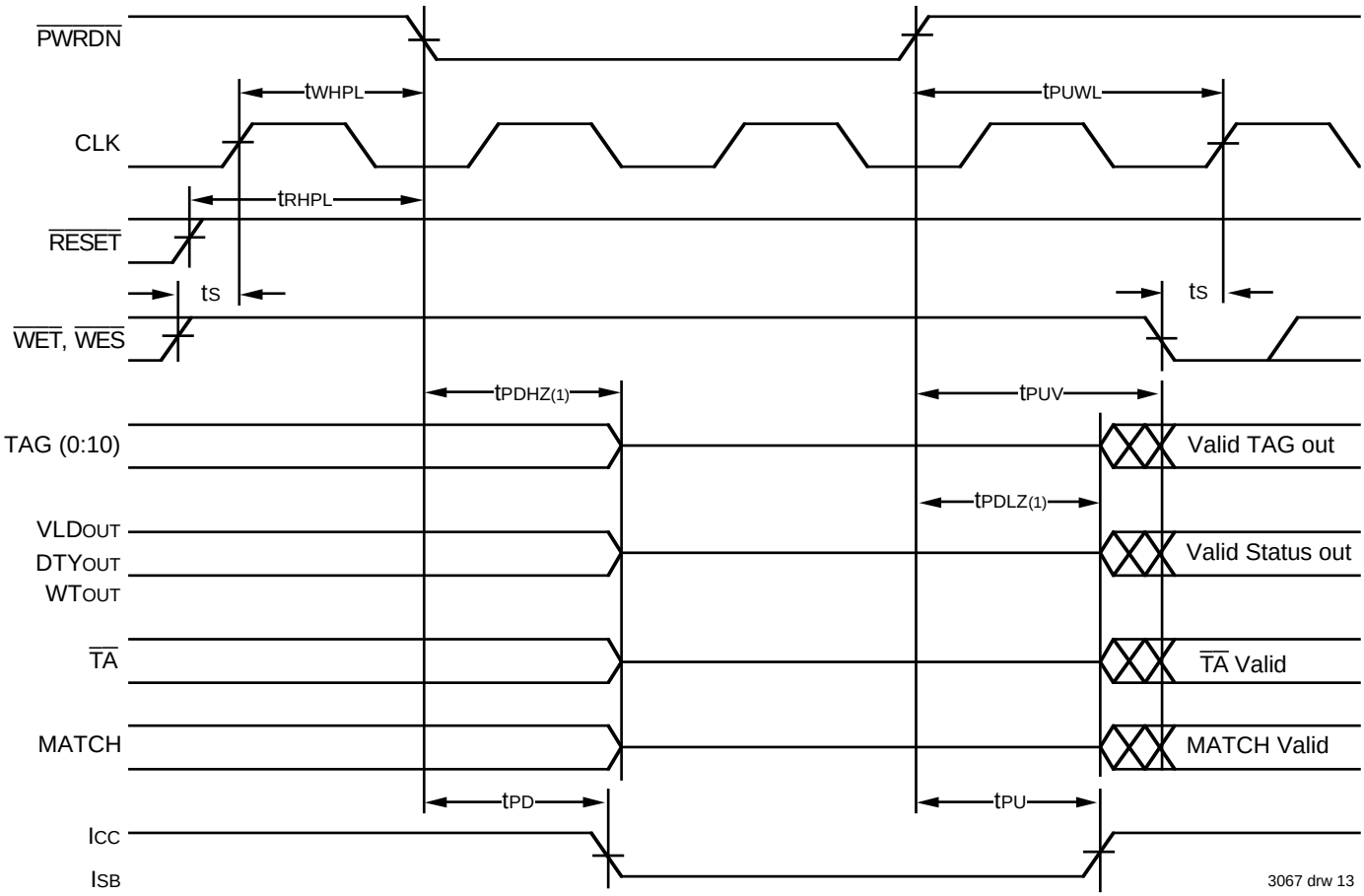


TIMING WAVEFORMS OF $\overline{OES}$ FUNCTION



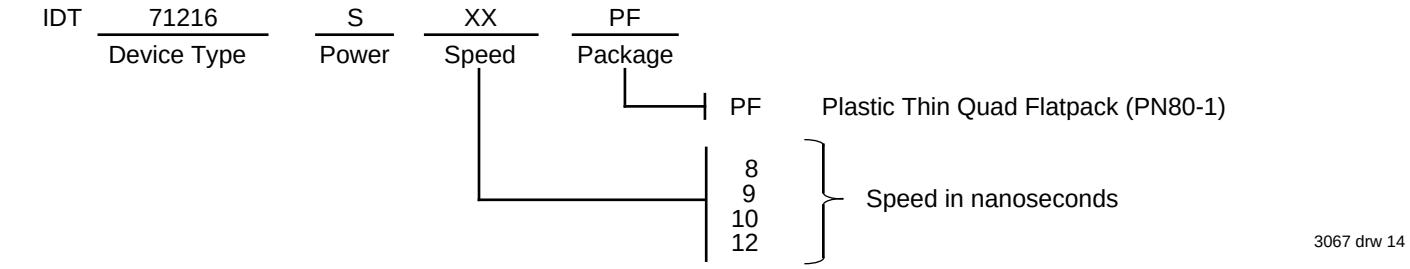
NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF POWER DOWN FUNCTION



NOTE:
1. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



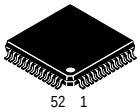
Low Voltage PLL Clock Driver

MPC970

LOW VOLTAGE PLL CLOCK DRIVER

The MPC970 is a 3.3V compatible, PLL based clock driver devices targeted for high performance RISC or CISC processor based systems.

- Fully Integrated PLL
- Output Frequency Up to 250MHz
- Compatible with PowerPC™ and Pentium™ Processors
- Output Frequency Configuration
- On–Board Crystal Oscillator
- 52–Lead TQFP Packaging
- ±50ps Typical Cycle–to–Cycle Jitter



FA SUFFIX
TQFP PACKAGE
CASE 848D–03

The MPC970 was designed specifically to drive today's PowerPC 601 and Pentium processors while providing the necessary performance to address higher frequency PowerPC 601 as well as PowerPC 603 and PowerPC 604 applications. The 2x_PCLK output can toggle at up to 250MHz while the remaining outputs can be configured to drive the other system clocks for MPC 601 based systems. As the processor based clock speeds increase the processor bus will likely run at one third or even one fourth the processor clock. The MPC970 supports the necessary waveforms to drive the BCLKEN input signal of the MPC 601 when the processor bus is running at a lower frequency than the processor. The MPC970 uses an advanced PLL design which minimizes the jitter generated on the outputs. The jitter specification is well within the requirements of the Pentium processor and meets the stringent preliminary specifications of the PowerPC 603 and PowerPC 604 processors. The application section of this data sheet deals in more detail with driving PowerPC and Pentium processor based systems.

The external feedback option of the MPC970 provides for a near zero delay between the reference clock input and the outputs of the device. This feature is required in applications where a master clock is being picked up off the backplane and regenerated and distributed on a daughter card. The advanced PLL of the MPC970 eliminates the dead zone of the phase detector and minimizes the jitter of the PLL so that the phase error variation is held to a minimum. This phase error uncertainty makes up a major portion of the part–to–part skew of the device.

For single clock driver applications the MPC970 provides an internal oscillator and internal feedback to simplify board layout and minimize system cost. By using the on–board crystal oscillator the MPC970 acts as both the clock generator and distribution chip. The external component is a relatively inexpensive crystal rather than a more expensive oscillator. Since in single board applications the delay between the input reference and the outputs is inconsequential an internal feedback option is offered. The internal feedback simplifies board design in that the system designer need not worry about noise being coupled into the feedback line due to board parasitics and layout. The internal feedback is a fixed divide by 32 of the VCO. This divide ratio ensures that the input crystals will be ≤20MHz, thus keeping the crystal costs down and ensuring availability from multiple vendors.

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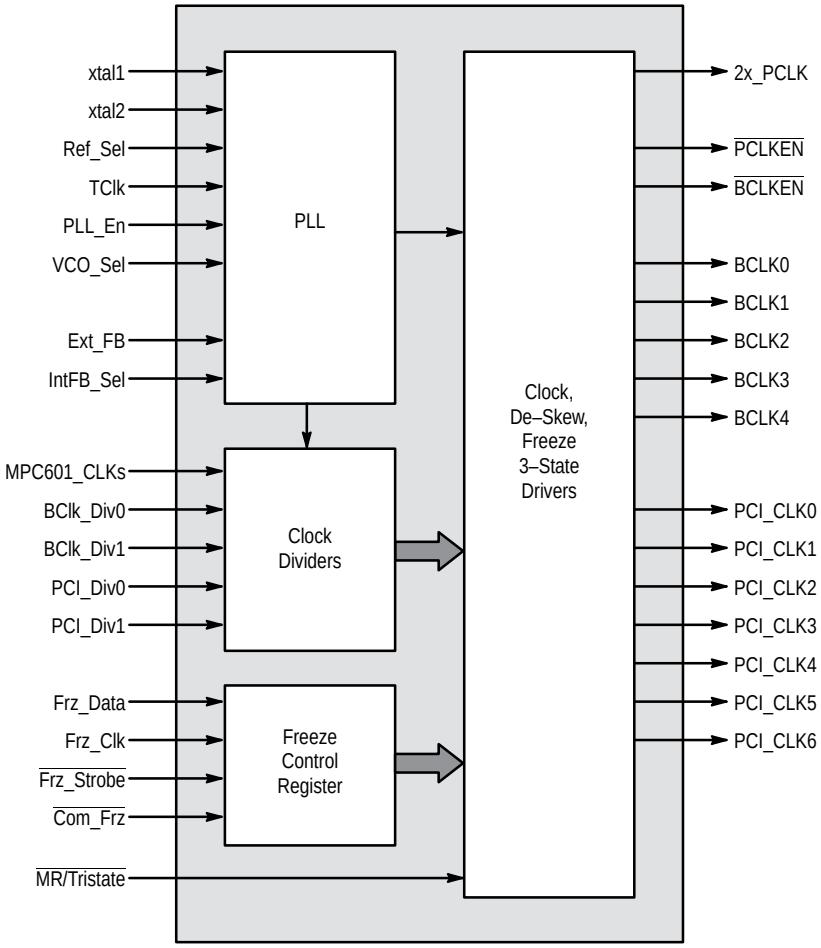
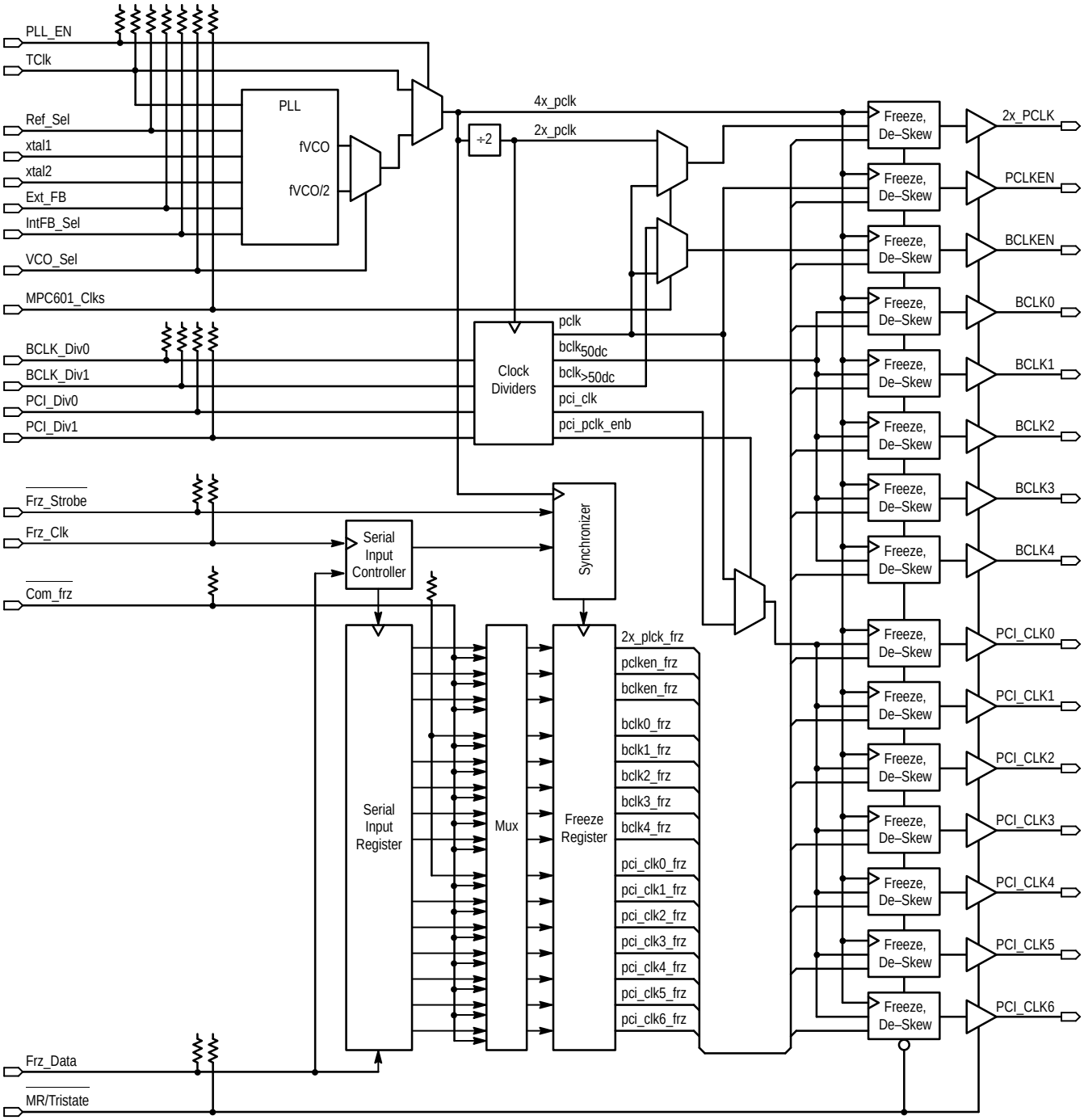


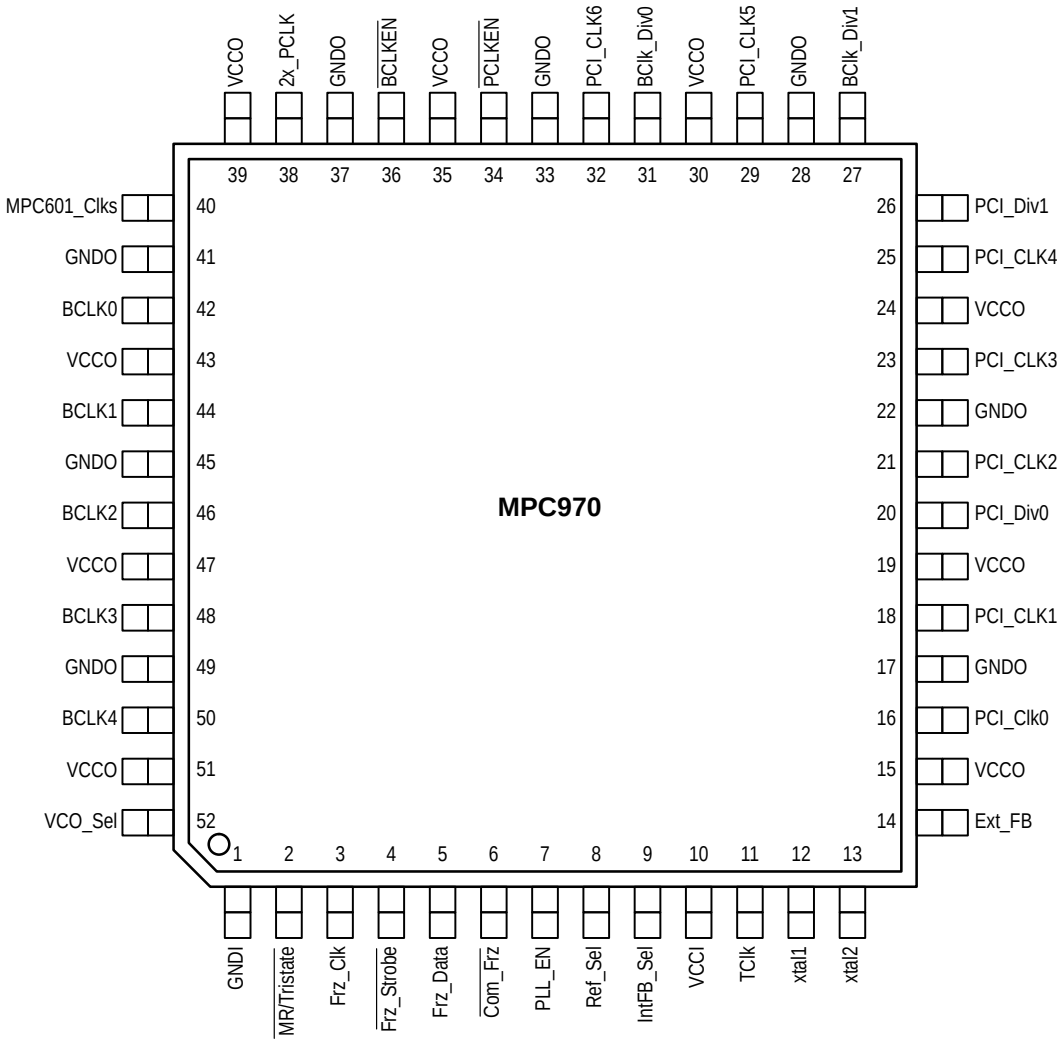
The MPC970 offers a very flexible output enable/disable scheme. This enable/disable scheme helps facilitate system debug as well as provide unique opportunities for system power down schemes to meet the requirements of “green” class machines. The MPC970 allows for the enabling of each output independently via a serial input port or a common enable/disable of all outputs simultaneously via a parallel control pin. When disabled or “frozen” the outputs will be locked in the “LOW” state, however the internal state machines will continue to run. Therefore when “unfrozen” the outputs will activate synchronous and in phase with those outputs which were not frozen. The freezing and unfreezing of outputs occurs only when they are already in the “LOW” state, thus the possibility of runt pulse generation is eliminated. A power–on reset will ensure that upon power up all of the outputs will be active.

For IC and board level testing a $\overline{\text{MR/Tristate}}$ input is provided. When pulled “LOW” all outputs will tristate and all internal flip flops will be reset. In addition the internal PLL can be bypassed and the fanout dividers and output buffers can be driven directly by the TClk input pin. Note that in this mode it will take a number of input clock pulses to cause output transitions as the TClk is fed through the internal dividers.

The MPC970 is fully 3.3V (3.6V for PowerPC 601 designs) compatible and requires no external loop filter components. All inputs accept LVCMOS/LVTTL compatible levels while the outputs provide LVCMOS levels with the capability to drive 50Ω transmission lines. For series terminated lines each MPC970 output can drive two 50Ω lines in parallel thus effectively doubling the fanout of the device.

SIMPLIFIED BLOCK DIAGRAM





FUNCTION TABLE 1

MPC601_Clks	2x_PCLK	PCLKEN	BCLKEN	BCLK	PCI_CLK
0	VCO/4	VCO/4	VCO/4	X	X
1	VCO/2	VCO/4	BCLK*	X	X

* Output is purposely delayed vs 2x_PCLK output.

FUNCTION TABLE 2

PCI_Div1	PCI_Div0	PCI_CLK	BCLK_Div1	BCLK_Div0	BCLK
0	0	BLCK	0	0	PCLKEN
0	1	BCLK/2	0	1	PCLKEN/2
1	0	BCLK/3	1	0	PCLKEN/3
1	1	PCLKEN	1	1	PCLKEN/4

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
VCO_Sel	fVCO/2	fVCO
Ref_Sel	TCLK	Crystal Osc
PLL_En	Bypass PLL	Enable PLL
IntFB_Sel	Ext Feedback	Int Feedback

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current	TBD	TBD	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic		Min	Max	Unit	Condition
V_{CC}	Power Supply Voltage		3.0	3.8	V	
I_{CC}	Quiescent Power Supply			250	mA	
V_{IL}	Input Voltage LOW	LVCMOS Inputs		$0.3V_{DD}$	V	
V_{IH}	Input Voltage HIGH	LVCMOS Inputs	$0.7V_{DD}$	TBD	V	
I_{IH}	Input Current HIGH	LVCMOS Inputs		–100	µA	$V_{IN} = V_{CC}$
I_{IL}	Input Current LOW		–200		µA	V_{IN} = GND
V_{OH}	Output Voltage HIGH		V_{DD}–0.2		V	I_{OH} = –20mA[1]
V_{OL}	Output Voltage LOW			0.2	V	I_{OL} = 20mA[1]
I_{OZ}	Tristate Output Leakage Current		–10	10	µA	$V_{OH} = V_{CC}$ or GND
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance				pF	
C_{OUT}	Output Capacitance			8	pF	

1. The MPC970 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	10	Note 1	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{Xtal}	Crystal Oscillator Frequency	10		25	MHz	Note 4
F_{out}[2]	Maximum 2x_PCLK Output Frequency			200	MHz	
t_{DC}[1,2]	Output Duty Cycle	45 35		55 65	%	F_{out} < 200MHz F_{out} ≥ 200MHz
V_{OH}AC	AC Output HIGH Voltage	2.4 2.2			V	F_{out} < 200MHz F_{out} ≥ 200MHz
V_{OL}AC	AC Output LOW Voltage			0.4 0.6	V	F_{out} < 200MHz F_{out} ≥ 200MHz
t_{pw}[1,2]	2x_PCLK Pulse Width	1.75	2.27		ns	F_{out} = 200MHz
t_{per}	Minimum Clock Out Period	4.85	4.91		ns	F_{out} = 200MHz
t_{pd}[3]	SYNC to Feedback Propagation Delay Feedback = VCO/4 Feedback = VCO/8 Feedback = VCO/12 Feedback = VCO/16 Feedback = VCO/24 Feedback = VCO/36 Feedback = VCO/48		X_1±150 X_2±150 X_3±150 X_4±150 X_5±150 X_6±150 X_7±150		ps	
f_{VCO}	VCO Lock Range Feedback = VCO/4 Feedback = VCO/8 Feedback = VCO/12 Feedback = VCO/16 Feedback = VCO/24 Feedback = VCO/32 Feedback = VCO/36 Feedback = VCO/36	 TBD TBD TBD TBD TBD TBD TBD TBD	 200–700 200–700 200–700 200–700 200–700 200–700 200–700 200–700	 TBD TBD TBD TBD TBD TBD TBD TBD	MHz	 Ext Feedback Ext Feedback Ext Feedback Ext or Int Feedback Ext Feedback Int Feedback Ext Feedback Ext Feedback
t_{jitter}[1,2]	Output Jitter		±50 110 76	±100 190 210	ps	PLL Jitter 2x_P Period Variation Period Variation (Other)
t_{skew}[1,2]	Output–to–Output Skew 2x_PCLCK, PCLKEN, BCLKEN, BCLK 2x_PCLK, PCLKEN, BCLK PCI_CLK BCLK All			 550 550 450 550 800	ps	 MPC601_Clks = ‘0’ MPC601_Clks = ‘1’
t_{delay}	Propagation Delay 2x_PCLK to BCLKEN	100		850	ps	MPC601_Clks = ‘1’
t_r, t_f[1,2]	Output Rise/Fall Time	0.15		1.5	ns	0.8 to 2.0V
t_{lock}	PLL Lock Time			10	ms	
t_{PZL}	Output Enable Time $\overline{MR/Tristate}$ to Outputs			8	ns	
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{MR/Tristate}$ to Outputs			10	ns	
f_{MAX}	Maximum Frz_Clk Frequency			20	MHz	
t_s	Setup Time Frz_Data to Frz_Clk $\overline{Com\_Frz}$ to $\overline{Frz\_Strobe}$	8 5				
t_h	Hold Time Frz_Clk to Frz_Data $\overline{Frz\_Strobe}$ to $\overline{Com\_Frz}$	8 5				

1. Measured at 1.4V.
2. Drive 50Ω transmission lines.
3. X_1, X_2, X_3, X_4, X_5, X_6, and X_7 all to be determined. The specs hold only when the 970 or 971 is used in the external feedback mode.
4. See Applications Info section for more crystal information.

DETAILED PIN DESCRIPTIONS

The following gives a brief description of the functionality of the MPC970 I/O. Unless explicitly stated all inputs are LVCMOS/LVTTL compatible with internal pull up resistors. All outputs are LVCMOS level outputs which are capable of driving two series terminated 50Ω transmission lines on the incident edge.

xtal1, xtal2

These input pairs are the pins which differentiate the MPC970 and the MPC971. For the MPC970 the xtal1 and xtal2 pins represent the external crystal connections to the internal oscillator. The crystal oscillator is completely self contained, there are no external components required. The oscillator is specified to function for crystals of up to 50MHz. Exact crystal specifications are outlined in the applications section.

VCO_Sel

The VCO_Sel pin allows the user to further divide the internal VCO frequency for the generation of lower frequencies at the outputs. The VCO_Sel pin should be used to set the VCO into its most optimum range. Refer to the applications section for more details on the VCO frequency range. A logic '1' on the VCO_Sel pin will bypass the internal ÷2.

TClk

The TClk input serves a dual purpose; it can be used as either a reference clock input for the PLL from an external frequency source or it can be used as a board level test clock in the PLL bypass mode.

PLL_En

The PLL_En pin allows the TClk input to be routed around the PLL for system test and debug. When pulled low the MPC970 will be placed in the test mode. Note that the TClk input will be routed through the divider chain. For instance in the PowerPC 601 microprocessor clock generation mode the TClk input will toggle twice for each toggle on the 2x_PCLK output. Depending on the states of the frequency divider select pins this ratio may be higher.

Frz_Data

Frz_Data is the serial data input for the output freeze function of the device. Refer to the applications section for more information on the freeze functionality.

Frz_Clk

Frz_Clk is the serial freeze logic clock input. Refer to the applications section for more information on the freeze functionality.

$\overline{\text{Frz\_Strobe}}$

The $\overline{\text{Frz\_Strobe}}$ input is used to freeze or unfreeze all of the outputs simultaneously. Refer to the applications section for more information on the freeze functionality.

$\overline{\text{Com\_Frz}}$

The $\overline{\text{Com\_Frz}}$ input allows the user to enable/disable all of the outputs with the control of a single pin. The action will take place upon a high to low transition of the $\overline{\text{Frz\_Strobe}}$ input.

BClk_Div0:1

The BClk_Div inputs are used to program the VCO divide ratio for the BCLK outputs. These inputs also set the divide ratio of the BCLKEN output to be equal in frequency to the BCLK outputs when the device is in the MPC601_Clks mode. The BClk_Div inputs set the frequency as follows:

BClk_Div1	BClk_Div0	BCLK Frequency
0	0	PCLKEN
0	1	PCLKEN/2
1	0	PCLKEN/3
1	1	PCLKEN/4

In most applications these inputs will be strapped to the appropriate power rails.

PCI_Div0:1

The PCI_Div inputs set the division ratio for the PCI_CLKs. The PCI_CLKs are set relative to the BCLK or the PCLKEN output such that you can upgrade the processor bus and maintain the PCI bus frequency in the currently defined ≤ 33MHz range. The PCI_Div inputs set the PCI_CLKs as follows:

PCI_Div1	PCI_Div0	PCI_CLK Frequency
0	0	BCLK
0	1	BCLK/2
1	0	BCLK/3
1	1	PCLKEN

In a typical application these inputs will be strapped to the appropriate power rail.

MPC601_Clks

The MPC601_Clks input will configure the outputs to drive the PowerPC 601 microprocessor when pulled HIGH or left open. When pulled LOW it will configure the 2xPCLK, PCLKEN and BCLKEN all into a VCO/4 mode. In this mode the MPC970 will have three more outputs available to drive clock loads on the processor bus for PowerPC 603, PowerPC 604 or Pentium microprocessor based systems.

Ext_FB

The Ext_FB pin is an input to the phase detector of the PLL which is tied to an external feedback output. Typically this feedback will be one of the lowest frequency outputs of the MPC970.

IntFB_Sel

The IntFB_Sel input selects whether the internal feedback signal or an external feedback signal is routed to the phase detector of the PLL. The default mode, pulled HIGH via the internal pull up resistor, is to select the internal feedback.

$\overline{\text{MR}}$/Tristate

The $\overline{\text{MR}}$/Tristate input when pulled LOW will reset all of the internal flip flops and also tristate all of the clock outputs. This input is used primarily for IC and board level test.

Ref_Sel

The Ref_Sel input allows the user to choose between two sources for the PLL reference frequency. For the MPC970, LOW on Ref_Sel will choose the LVCMOS TCLK input. For the MPC970, a HIGH on Ref_Sel will choose the crystal oscillator input.

2x_PCLK

In general the outputs are named based on the implementation in a PowerPC 601 microprocessor based system. In the MPC601_Clk mode the 2x_PCLK will run at half the internal VCO frequency. With a maximum internal VCO frequency of 1000MHz this output could theoretically toggle at 500MHz, in practice however the output can toggle only as fast as 300MHz. This frequency will be required on future enhancements to the MPC 601 microprocessor. When the MPC970 is taken out of the MPC601_Clk mode the 2xPCLK will run at a VCO/4 frequency. This divide ratio will place this output frequency in the present and future processor bus speeds of the PowerPC 603, PowerPC 604 and Pentium microprocessors. The 2x_PCLK output is a 50% duty cycle LVCMOS output.

PCLKEN

The PCLKEN output is designed to drive the PCLKEN input of the PowerPC 601 microprocessor when the MPC970 is in the MPC601_Clk mode. The PCLKEN output frequency is one half that of the 2x_PCLK output, a divide by four of the internal VCO. The PCLKEN output runs at the same frequency regardless of the state of the frequency divide controls. The toggle frequency of this output is well placed for driving the PowerPC 603, PowerPC 604 and Pentium processor buses. The PCLKEN output is a 50% duty cycle LVCMOS output.

BCLKEN

The BCLKEN output is designed to drive the BCLKEN input of the PowerPC 601 microprocessor when the MPC970 is in the MPC601_Clks mode. The BCLKEN toggles at the same frequency as the BCLK outputs as described earlier. However when the BCLKEN output is a divide by three or a divide by four of the PCLKEN output the duty cycle is 66/33 and 75/25 respectively per the requirement of the MPC 601 processor. In addition to meet the HOLD time spec for the BCLKEN input of the MPC 601 the BCLKEN output of the MPC970 lags the 2xPCLK output by no less than 100ps. When the MPC970 is not in the MPC601_Clks mode the BCLKEN output is set at a fixed divide by four from the internal VCO. In addition in this mode the BCLKEN output does NOT lag the other outputs, but rather is synchronous within the Output–to–Output skew spec of the device.

BCLK0:4

The BCLK outputs are designed to drive the clock loads on the processor bus of either the PowerPC or Pentium microprocessors. The most common practice in “non MPC 601” applications will be to place these outputs in the PCLKEN/1 mode and combine them with the above outputs to drive all of the loads on the processor bus. The division ratios do allow for the swap of these outputs with the PCI_CLK outputs if more clocks are needed to drive the processor bus. For PowerPC 601 microprocessor based systems the division ratios allow the processor internal speeds to be increased while maintaining reasonable speeds for the L2 cache and the PCI bridge chip. The BCLK outputs are 50% duty cycle LVCMOS outputs.

PCI_Clk0:6

As the name would suggest the PCI_CLK outputs are designed to drive the PCI bus clock loads in a typical microprocessor based system. The division ratios allow for these outputs to remain in the ≤ 33MHz PCI bus speeds for various common processor bus speeds as well as higher future processor bus speeds. These outputs can also be programmed to run at the processor bus speeds if more processor bus clocks are required. The PCI_CLK outputs are 50% duty cycle LVCMOS outputs.

APPLICATIONS INFORMATION

Programming the MPC970

The MPC970 is very flexible in the programming of the frequency relationships of the various outputs as well as the relationships between the input references and outputs. The purpose of this section is to outline the various relationships. Although not exhaustive the hope is that enough information is supplied to allow the customers to tailor the I/O relationships for their specific applications.

The VCO used in the MPC970 is a differential ring oscillator. The VCO exhibits a very wide frequency range to allow for a great deal of flexibility to the end user. Special design techniques were used in the overall PLL design to keep the relatively high gain of the VCO from significantly impacting the jitter of the PLL.

Table 1 tabulates the various output frequencies for the different modes defined by the division select input pins. In this table the VCO_Sel pin is high so that the ÷2 prescaler is bypassed. Note that the ÷32 feedback is always fed directly from the VCO and is thus unaffected by the level on the VCO_Sel input. Table 1 shows each of the output frequencies as a function of the VCO frequency. The two VCO ranges can be used to plug in values to get the actual frequencies. When the internal feedback option is used the multiplication factor of the device will equal 32 divided by the

output divide ratio. If the VCO_Sel pin is “LOW” the multiplication factor will be reduced further by 2. (See “Using the On–Board Crystal Oscillator” section of this datasheet.)

Using the External Feedback Feature of the MPC970/71

In applications where the relationship between the output waveforms and the input waveforms are critical the external feedback option will likely be used. Table 1 and Table 2 are still appropriate for establishing the potential output frequency relationships. The input reference frequency for external feedback applications will be equal to the frequency of the feedback signal. As a result the use of the external feedback yields a number of potential input to output frequency multiplication factors which are not available using the internal feedback. Using the external feedback the device can function as a zero delay buffer and could multiply the input from 4 to as much as 48. In practice however the multiplication factor is limited by the loop dynamics of the PLL. The MPC970 PLL was optimized for an input reference frequency or greater than 10MHz. Frequencies lower than 10MHz will tend to pass through the filter and add jitter to the PLL. In addition the PLL was optimized for feedback divide ratios of between 8 and 64. The user should avoid using the device with feedback divide ratios outside of this range. For the external feedback case the feedback divide ratio will include the ÷2 (if VCO_Sel is LOW) plus the output divider for the feedback output. If, for instance the MPC970 is to be used as a zero delay buffer the VCO_Sel pin should be pulled LOW and all of the outputs should be set in a VCO/4 mode. This would produce a feedback ratio of ÷8. Several potential configurations using the external feedback are pictured in Figure 1 through Figure 4.

The external feedback option of the MPC970 is critical for applications in which more than one clock driver need to be synchronized. The external feedback option ensures that the feed through delay is the same as the feedback delay. This functionality removes propagation delay variation as a factor in the determination of part to part skew. The low jitter PLL used in the MPC970 has a near zero deadband phase detector and very little part to part variability. The result is a very low phase error variability in the product. When coupled with the output to output skew the phase error variability accounts for the part to part skew of the device. From the specification table one sees that the worst case part to part skew of the device is 800ps, assuming that there is zero skew in the multiple reference inputs. For multiple MPC970 applications if the lowest generated output frequency is used as the feedback signal the devices will be guaranteed to be synchronized. For applications where the lowest frequency is not used as the reference or where the internal feedback is used there is no way to guarantee that the multiple devices will be phase synchronized.

Table 1. Programmable Output Frequency Relationships (MPC601_Clks = ‘HIGH’; VCO_Sel = ‘HIGH’)

INPUTS				OUTPUTS				
PCI_Div1	**PCI_Div0**	**BCLK_Div1**	**BCLK_Div0**	**2x_PCLK**	**PCLKEN**	**BCLKEN***	**BCLK**	**PCI_CLK**
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/12
0	0	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/16
0	1	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/8
0	1	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/16
0	1	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/24
0	1	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/32
1	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/12
1	0	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/24
1	0	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/36
1	0	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/48
1	1	0	0	VCO/2	VCO/4	VCO/4	VCO/4	VCO/4
1	1	0	1	VCO/2	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	0	VCO/2	VCO/4	VCO/12	VCO/12	VCO/4
1	1	1	1	VCO/2	VCO/4	VCO/16	VCO/16	VCO/4

* BCLK_En output is delayed relative to other outputs

Table 2. Programmable Output Frequency Relationships (MPC601_Clks = 'LOW'; VCO_Sel = 'HIGH')

INPUTS				OUTPUTS				
PCI_Div1	**PCI_Div0**	**BCLK_Div1**	**BCLK_Div0**	**2x_PCLK**	**PCLKEN**	**BCLKEN***	**BCLK**	**PCI_CLK**
0	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/8
0	0	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/12
0	0	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/16
0	1	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/8
0	1	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/16
0	1	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/24
0	1	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/32
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/12
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/24
1	0	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/36
1	0	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/48
1	1	0	0	VCO/4	VCO/4	VCO/4	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/4	VCO/4	VCO/8	VCO/4
1	1	1	0	VCO/4	VCO/4	VCO/4	VCO/12	VCO/4
1	1	1	1	VCO/4	VCO/4	VCO/4	VCO/16	VCO/4

* BCLK_En output is coincident with other outputs

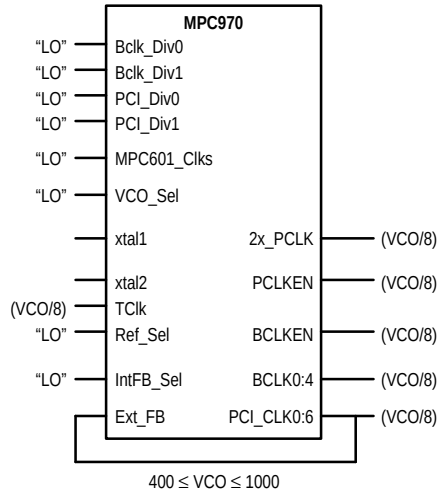


Figure 1. External Feedback Configuration 1

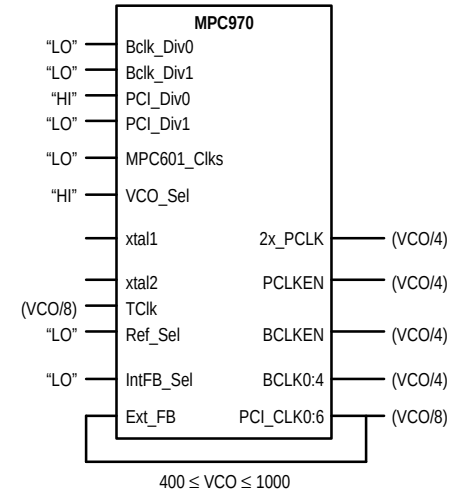


Figure 2. External Feedback Configuration 2

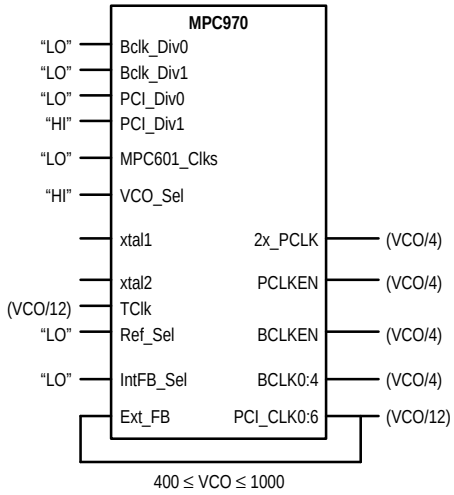


Figure 3. External Feedback Configuration 3

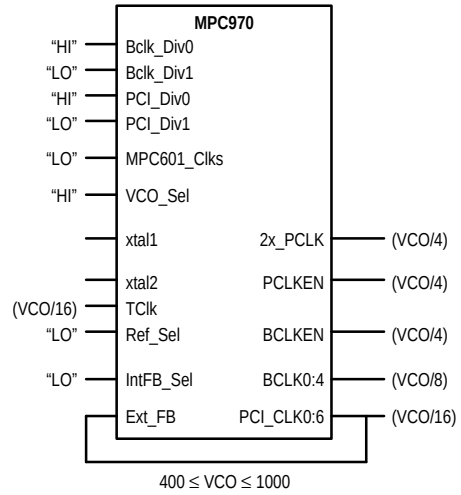


Figure 4. External Feedback Configuration 4

Using the On–Board Crystal Oscillator

The MPC970 features an on–board crystal oscillator to allow for seed clock generaytion as well as final distribution. The on–board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC970 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required. In addition, with crystals with a higher shunt capacitance, it may be necessary to place a 1k resistor across the two crystal leads.

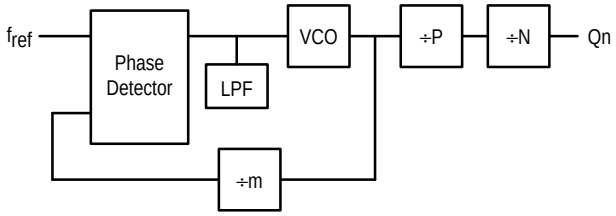
The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on–board capacitors. Because the design is a series resonant design for the optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC970 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Table 3. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental at Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100µW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

The MPC970 is a clock driver which was designed to generate outputs with programmable frequency relationships and not a synthesizer with a fixed input frequency. As a result the crystal input frequency is a function of the desired output frequency. For a design which utilizes the external feedback to the PLL the selection of the crystal frequency is straight forward; simply chose a crystal which is equal in frequency to the fed back signal. To determine the crystal required to produce the desired output frequency for an application which utilizes internal feedback the block diagram of Figure 5 should be used. The P and the M values for the MPC970 are also included in Figure 5. The M values can be found in the configuration tables included in this applications section.



$$f_{ref} = \frac{f_{VCO}}{m}, \quad f_{VCO} = fQn \cdot N \cdot P$$

$$\therefore\ f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

m = 32
P = 1 (VCO_Sel=‘1’), 2(VCO_Sel=‘0’)

Figure 5. PLL Block Diagram

For the MPC970 clock driver, the following will provide an example of how to determine the crystal frequency required for a given design.

Given:

2x_PCLK = 200MHz
PCLKEN = 100MHz
BCLK = 50MHz
PCI_CLK = 25MHz
VCO_SEL = ‘1’

$$f_{ref} = \frac{fQn \cdot N \cdot P}{m}$$

From Table 3

PCI_CLK = VCO/16 then N = 16
or
PCLKEN = VCO/4 then N = 4

From Figure 5

m = 32 and P = 1

$$f_{ref} = \frac{25 \cdot 16 \cdot 1}{32} = 12.5\text{MHz} \text{ or } \frac{100 \cdot 4 \cdot 1}{32} = 12.5\text{MHz}$$

Driving Transmission Lines

The MPC970 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel

terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC970 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC970 clock driver is effectively doubled due to its capability to drive multiple lines.

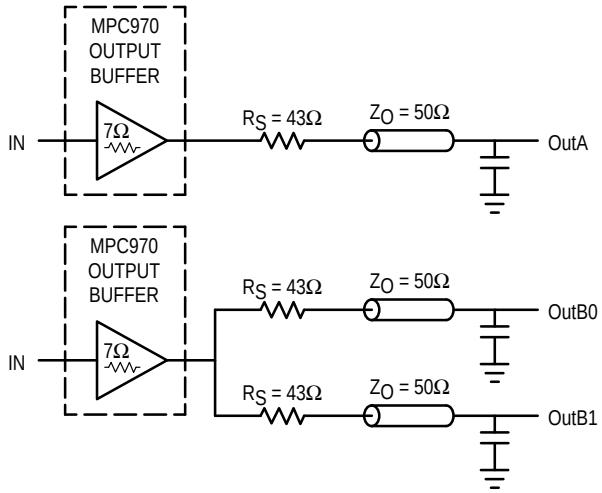


Figure 6. Single versus Dual Transmission Lines

The waveform plots of Figure 7 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC970 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC970. The output waveform in Figure 7 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

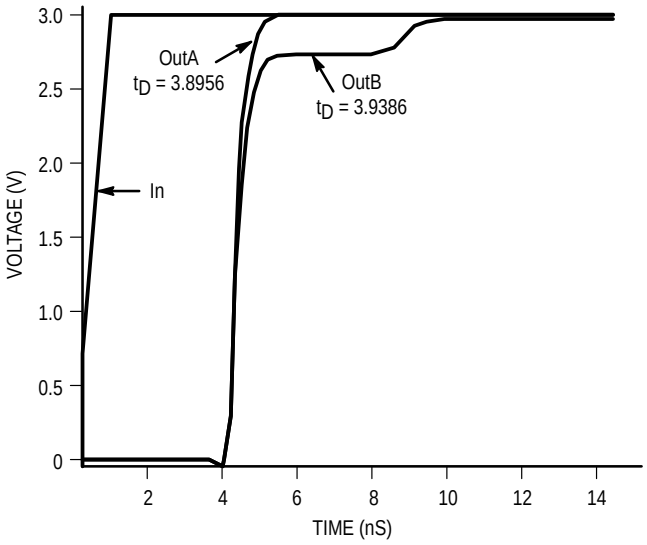
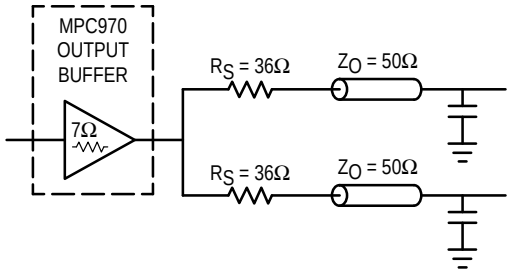


Figure 7. Single versus Dual Waveforms



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 8. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Using the Output Freeze Circuitry

With the recent advent of a “green” classification for computers the desire for unique power management among system designers is keen. The individual output enable control of the MPC970 allows designers, under software control, to implement unique power management schemes into their designs. Although useful, individual output control at the expense of one pin per output is too high, therefore a simple serial interface was derived to economize on the control pins.

The freeze control logic provides two mechanisms through which the MPC970 clock outputs may be frozen (stopped in the logic ‘0’ state):

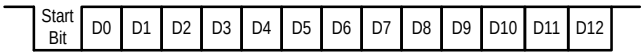
The first freeze mechanism allows serial loading of the 13–bit Serial Input Register, this register contains one programmable freeze enable bit for 13 of the 15 output clocks. The BCLK0 and PCI_CLK0 outputs cannot be frozen with the serial port, this avoids any potential lock up situation

should an error occur in the loading of the Serial Input Register. The user may programmably freeze an output clock by writing logic ‘0’ to the respective freeze enable bit. Likewise, the user may programmably unfreeze an output clock by writing logic ‘1’ to the respective enable bit.

The second freeze mechanism allows all 15 clocks to be frozen simultaneously by placing a logic ‘0’ on the $\overline{\text{Com\_Frz}}$ input and then issuing a low going pulse on the $\overline{\text{Frz\_Strobe}}$ input. Likewise, all 15 clocks can be simultaneously unfrozen by placing logic ‘1’ on the $\overline{\text{Com\_Frz}}$ input and then issuing a low–going pulse on the $\overline{\text{Frz\_Strobe}}$ input. Note that all 15 clocks are affected by the $\overline{\text{Frz\_Strobe}}$ freeze logic.

The freeze logic will never force a newly–frozen clock to a logic ‘0’ state before the time at which it would normally transition there. The logic simply keeps the frozen clock at logic ‘0’ once it is there. Likewise, the freeze logic will never force a newly–unfrozen clock to a logic ‘1’ state before the time at which it would normally transition there. The logic re–enables the unfrozen clock during the time when the respective clock would normally be in a logic ‘0’ state, eliminating the possibility of ‘runt’ clock pulses.

The user may write to the Serial Input register through the Frz_Data input by supplying a logic ‘0’ start bit followed serially by 13 NRZ freeze enable bits. After the 13th freeze enable bit the Frz_Data signal must be left in (or returned to) a logic ‘1’ state (Figure 9). The period of each Frz_Data bit equals the period of the free–running Frz_Clk signal. The Frz_Data serial transmission should be timed so the MPC970 can sample each Frz_Data bit with the rising edge of the free–running Frz_Clk signal.



D0 is the control bit for 2x_PCLK
D1 is the control bit for PCLKEN
D2 is the control bit for BCLKEN
D3–D6 are the control bits for BCLK1–BCLK4
D7–D12 are the control bits for PCI_CLK1–PCI_CLK6

Figure 9. Freeze Data Input Protocol

The user can combine the two freeze capabilities to simplify system level implementation. The serial input port can be used to establish the freeze mask to disable the appropriate outputs. The Frz_Strobe input can then be used to unfreeze the outputs without having to serially load an “all unfrozen” freeze mask.

Driving the PowerPC 601 Microprocessor

The MPC601 processor requires three clock inputs from the MPC970 clock driver. A 2x_PCLK input at twice the internal MPC 601 clock rate and the PCLKEN and BCLKEN signals used to mask internal clock edges. The PCLKEN signal always runs at one half the 2x_PCLK signal while the BCLKEN signal can run at 1x, 1/2x, 1/3x or 1/4x the PCLK input signal depending on the speed of the processor bus. When the BCLKEN signal is running at 1/3 or 1/4 the PCLK input the input duty cycle must be 66/33 and 75/25 respectively. In addition, as shown in Figure 10, to satisfy the BCLKEN to 2x_PCLK Hold specification the BCLKEN signal must be at least coincident with the 2x_PCLK edge. To simplify board level implementation it would be desirable that the BCLKEN signal actually lag the 2x_PCLK by a few hundred picoseconds. The MPC970 insures that its BCLKEN output always lags the 2x_PCLK input by at least 300ps.

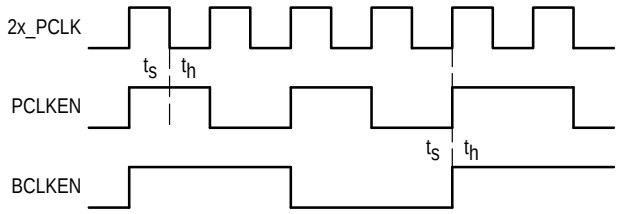


Figure 10. MPC601 Setup and Hold Times

Table 4 illustrates some typical MPC 601 system frequencies which can be realized using the MPC970 clock driver.

Table 4. Common MPC601 System Frequencies

2x_PCLK	PCLK	BCLK	PCI_CLK
240	120	60(1/2x)	30(1/2x)
240	120	40(1/3x)	20(1/2x)
240	120	30(1/4x)	30(1x)
200	100	50(1/2x)	25(1/2x)
200	100	33(1/3x)	33(1x)
200	100	25(1/4x)	25(1x)
160	80	40(1/2x)	20(1/2x)
160	80	20(1/4x)	20(1x)
132	66	66(1x)	33(1/2x)
132	66	33(1/2x)	33(1x)

Driving the PowerPC 603, PowerPC 604 and Pentium Microprocessors

The PowerPC 603, PowerPC 604 and Pentium processors differ from the MPC 601 processor in that the processor input clocks are at the same frequency as the processor bus. A typical system for these processors will include 8 – 16 clock loads on the processor bus. When the MPC970 is taken out of the MPC601_Clk mode there are a total of 8 “non PCI_CLK” outputs which can be run at the processor bus speeds for these microprocessors. Since each output can drive two series terminated transmission lines the MPC970 can support point to point clock distribution for up to 16 loads on the processor bus. In addition there will be 7 PCI_CLK outputs which can drive up to 14 loads on the PCI bus.

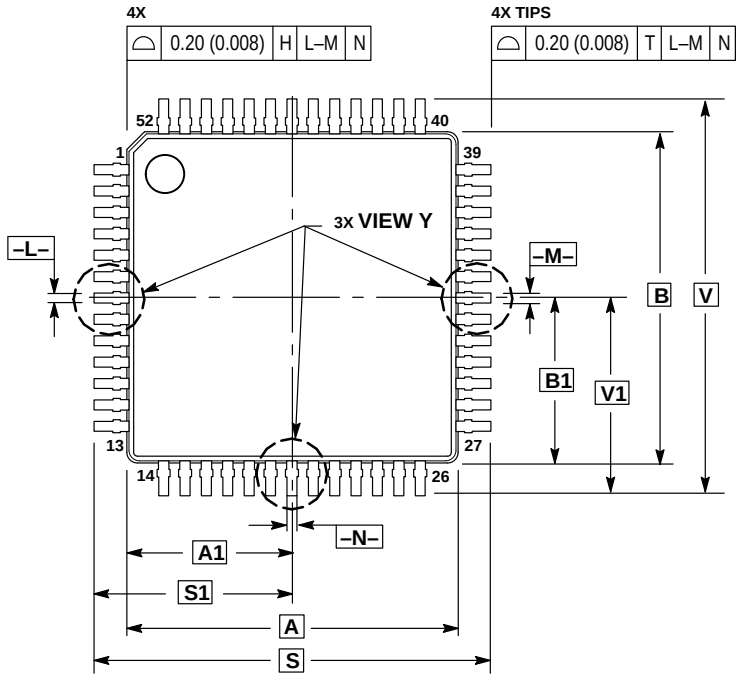
If more clock loads are present on the processor bus the PCI_CLKs can be configured to drive processor bus clock loads in addition to the BCLKs or alternatively the clocking roles of the BCLKs and PCI_CLKs can be reversed. Table 3 illustrates some useful frequency combinations for driving PowerPC 603, PowerPC 604 or Pentium microprocessor based systems.

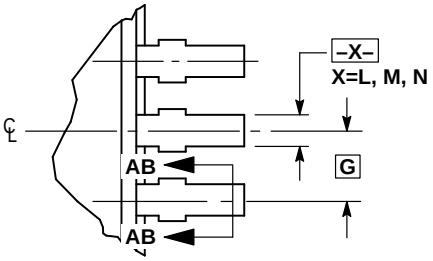
Table Table 5. Common PowerPC 603, PowerPC 604 and Pentium System Frequencies

2x_PCLK	PCLK	BCLK	PCI_CLK
80	80	80(1x)	26(1/3x)
75	75	75(1x)	25(1/3x)
66	66	66(1x)	33(1/2x)
66	66	66(1x)	66(1x)
66	66	33(1/2x)	66(PCLKEN)
60	60	60(1x)	30(1/2x)

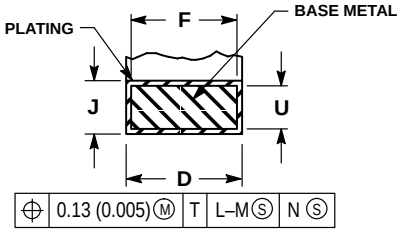
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D–03
ISSUE C

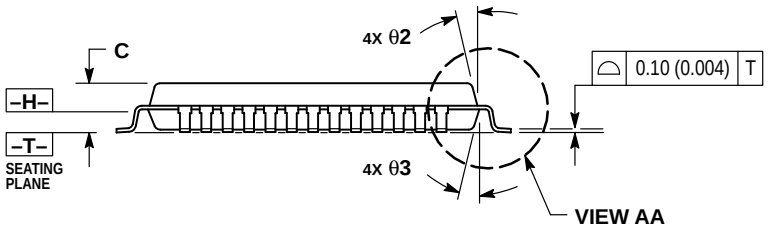


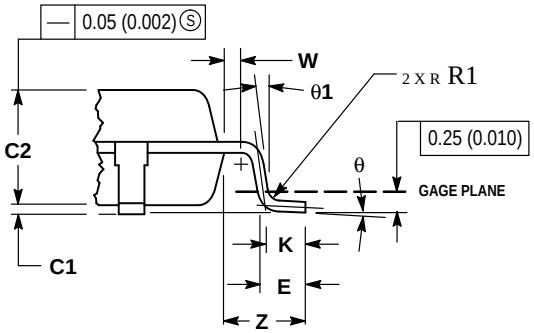


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

How to reach us:
USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

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- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
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- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
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- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
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- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
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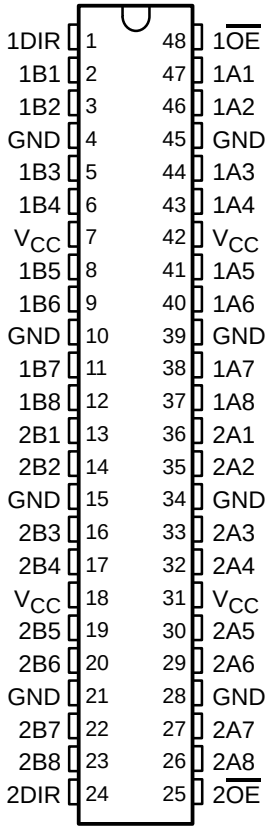
SN54LVTH16245A . . . WD PACKAGE
SN74LVTH16245A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVTH16245A are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the devices so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5-V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5-V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

description (continued)

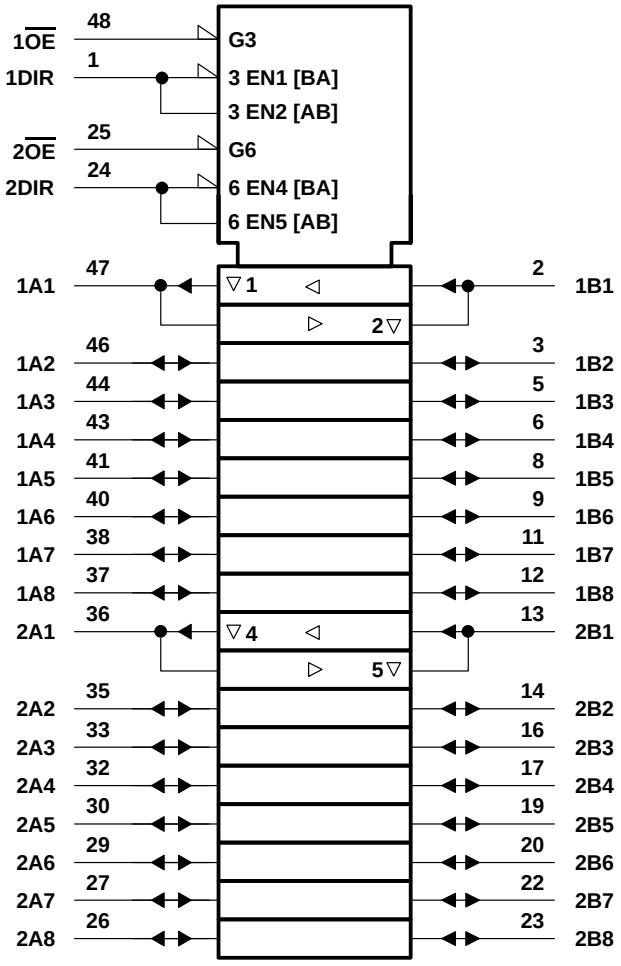
The SN74LVTH16245A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVTH16245A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16245A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

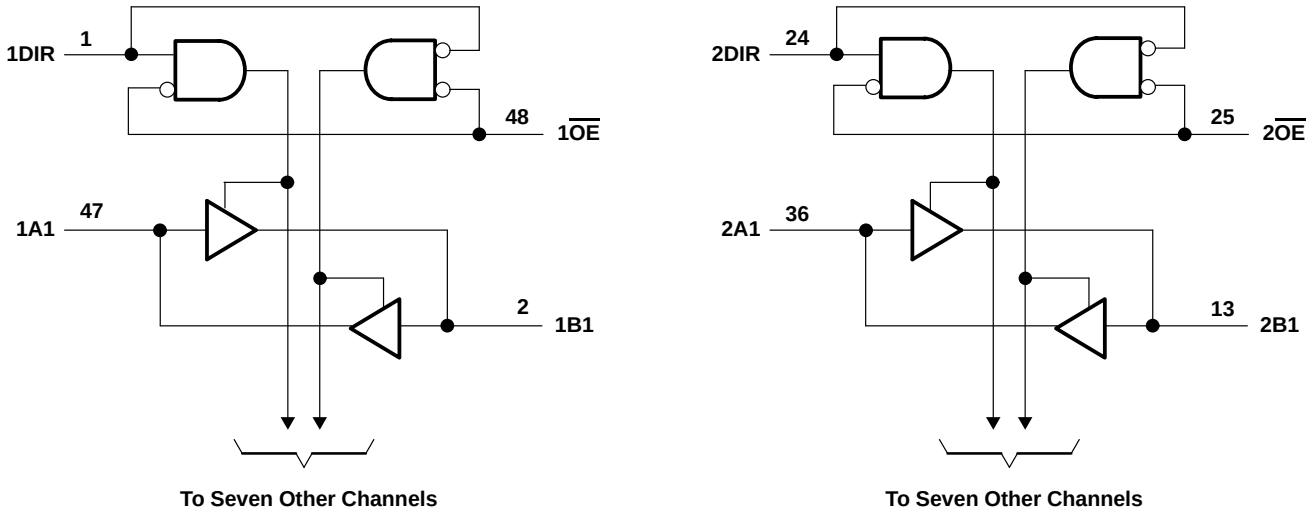
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTH16245A . . . . . 96 mA
SN74LVTH16245A . . . . . 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16245A . . . . . 48 mA
SN74LVTH16245A . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package . . . . . 0.85 W
DL package . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			SN54LVTH16245A		SN74LVTH16245A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTH16245A			SN74LVTH16245A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = –8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = –24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control inputs			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		V_I = V_{CC}				1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZPU}¶	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0			±100			±100	µA
I_{OZPD}¶	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0			±100			±100	µA
I_{CC}#	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high				0.19			0.19	mA
		Outputs low				5			5	
		Outputs disabled				0.19			0.19	
ΔI_{CC}	V_{CC} = 3 V to 3.6, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_{io}	V_O = 3 V or 0				10			10		pF

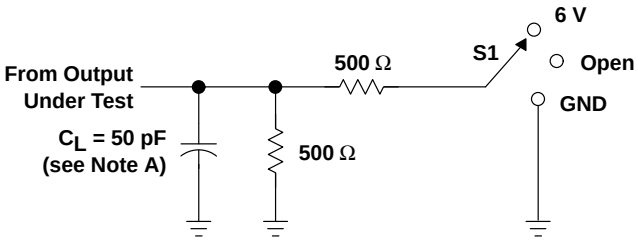
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This parameter is warranted by characterization but not production tested.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16245A				SN74LVTH16245A				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	A or B	B or A	1.5	3.5		3.9	1.5	2.3	3.3	3.7	ns
t_{PHL}			1.3	3.5		3.7	1.3	2.1	3.3	3.5	
t_{PZH}	$\overline{OE}$	A or B	1.5	4.8		5.6	1.5	2.8	4.5	5.3	ns
t_{PZL}			1.6	4.8		5.4	1.6	2.9	4.6	5.2	
t_{PHZ}	$\overline{OE}$	A or B	2.3	5.5		5.8	2.3	3.7	5.1	5.5	ns
t_{PLZ}			2.2	5.5		5.7	2.2	3.5	5.1	5.4	

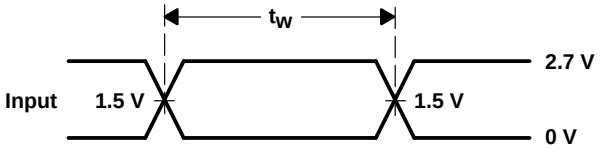
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

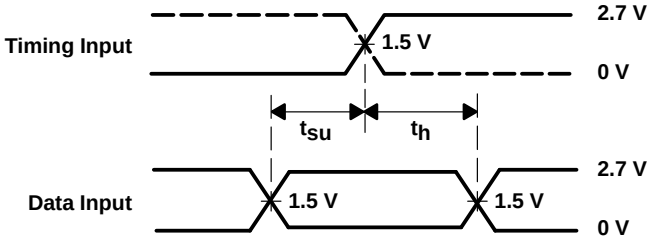


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

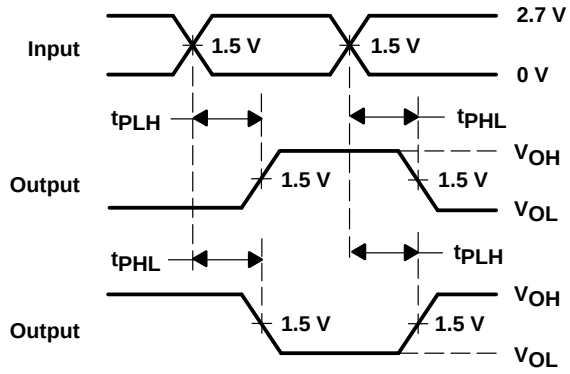
LOAD CIRCUIT



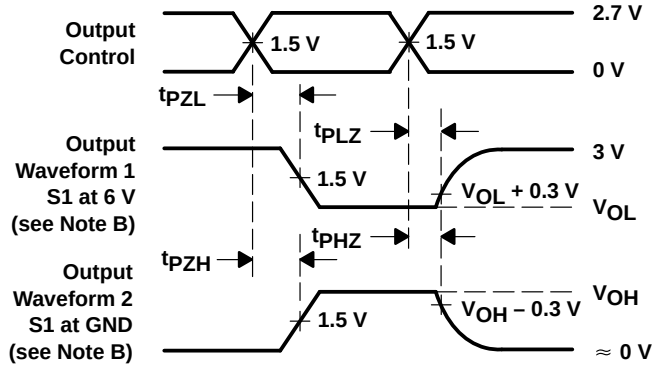
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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